



National Library
of Canada

Acquisitions and
Bibliographic Services Branch

395 Wellington Street
Ottawa, Ontario
K1A 0N4

Bibliothèque nationale
du Canada

Direction des acquisitions et
des services bibliographiques

395, rue Wellington
Ottawa (Ontario)
K1A 0N4

Your file Votre référence

Our file Notre référence

NOTICE

The quality of this microform is heavily dependent upon the quality of the original thesis submitted for microfilming. Every effort has been made to ensure the highest quality of reproduction possible.

If pages are missing, contact the university which granted the degree.

Some pages may have indistinct print especially if the original pages were typed with a poor typewriter ribbon or if the university sent us an inferior photocopy.

Reproduction in full or in part of this microform is governed by the Canadian Copyright Act, R.S.C. 1970, c. C-30, and subsequent amendments.

AVIS

La qualité de cette microforme dépend grandement de la qualité de la thèse soumise au microfilmage. Nous avons tout fait pour assurer une qualité supérieure de reproduction.

S'il manque des pages, veuillez communiquer avec l'université qui a conféré le grade.

La qualité d'impression de certaines pages peut laisser à désirer, surtout si les pages originales ont été dactylographiées à l'aide d'un ruban usé ou si l'université nous a fait parvenir une photocopie de qualité inférieure.

La reproduction, même partielle, de cette microforme est soumise à la Loi canadienne sur le droit d'auteur, SRC 1970, c. C-30, et ses amendements subséquents.

UNIVERSITY OF ALBERTA

**MICROMACHINED SERIAL TAPS IN
SILICON V-GROOVE WAVEGUIDES**

BY

KENNETH JOHN MACLEOD



A thesis submitted to the Faculty of Graduate Studies and Research in partial fulfillment of the requirements for the degree of **MASTER OF SCIENCE**.

DEPARTMENT OF ELECTRICAL ENGINEERING

EDMONTON, ALBERTA

FALL 1995



National Library
of Canada

Acquisitions and
Bibliographic Services Branch

395 Wellington Street
Ottawa, Ontario
K1A 0N4

Bibliothèque nationale
du Canada

Direction des acquisitions et
des services bibliographiques

395, rue Wellington
Ottawa (Ontario)
K1A 0N4

Your file *Votre référence*

Our file *Notre référence*

THE AUTHOR HAS GRANTED AN
IRREVOCABLE NON-EXCLUSIVE
LICENCE ALLOWING THE NATIONAL
LIBRARY OF CANADA TO
REPRODUCE, LOAN, DISTRIBUTE OR
SELL COPIES OF HIS/HER THESIS BY
ANY MEANS AND IN ANY FORM OR
FORMAT, MAKING THIS THESIS
AVAILABLE TO INTERESTED
PERSONS.

L'AUTEUR A ACCORDE UNE LICENCE
IRREVOCABLE ET NON EXCLUSIVE
PERMETTANT A LA BIBLIOTHEQUE
NATIONALE DU CANADA DE
REPRODUIRE, PRETER, DISTRIBUER
OU VENDRE DES COPIES DE SA
THESE DE QUELQUE MANIERE ET
SOUS QUELQUE FORME QUE CE SOIT
POUR METTRE DES EXEMPLAIRES DE
CETTE THESE A LA DISPOSITION DES
PERSONNE INTERESSEES.

THE AUTHOR RETAINS OWNERSHIP
OF THE COPYRIGHT IN HIS/HER
THESIS. NEITHER THE THESIS NOR
SUBSTANTIAL EXTRACTS FROM IT
MAY BE PRINTED OR OTHERWISE
REPRODUCED WITHOUT HIS/HER
PERMISSION.

L'AUTEUR CONSERVE LA PROPRIETE
DU DROIT D'AUTEUR QUI PROTEGE
SA THESE. NI LA THESE NI DES
EXTRAITS SUBSTANTIELS DE CELLE-
CI NE DOIVENT ETRE IMPRIMES OU
AUTREMENT REPRODUITS SANS SON
AUTORISATION.

ISBN 0-612-06504-9

Canada

University of Alberta

Release Form

NAME OF AUTHOR: **KENNETH JOHN MACLEOD**

TITLE OF THESIS: **MICROMACHINED SERIAL TAPS IN
SILICON V-GROOVE WAVEGUIDES**

DEGREE: **MASTER OF SCIENCE**

YEAR THIS DEGREE GRANTED: **1995**

Permission is hereby granted to the University of Alberta Library to reproduce single copies of this thesis and to lend or sell such copies for private, scholarly or scientific research purposes only.

The author reserves all other publication and other rights in association with the copyright in the thesis, and except as hereinbefore provided neither the thesis nor any substantial portion thereof may be printed or otherwise reproduced in any material form whatever without the author's prior written permission.

Ken MacLeod

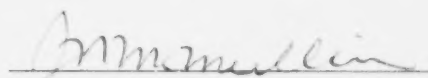
Kenneth John MacLeod
2365 Whitehaven Cr.,
Ottawa, Ontario
K2B 5H2

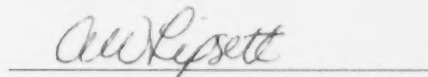
Date: 95/09/24

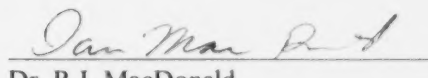
UNIVERSITY OF ALBERTA

FACULTY OF GRADUATE STUDIES AND RESEARCH

The undersigned certify that they have read, and recommend to the Faculty of Graduate Studies and Research for acceptance, a thesis entitled "**MICROMACHINED SERIAL TAPS IN SILICON V-GROOVE WAVEGUIDES**" submitted by **KENNETH JOHN MACLEOD** in partial fulfillment of the requirements for the degree of **MASTER OF SCIENCE**.


Dr. J.N. McMullin, Supervisor


Dr. A.W. Lipsett


Dr. R.I. MacDonald

Date: 95/09/23

ABSTRACT

Methods of fabricating serial out-of-plane taps in polymer waveguides are investigated.. The waveguides are formed in {111} v-grooves etched in silicon wafers. The taps, made up of silicon crystal planes, are micromachined inside the v-grooves. A computer program using ray tracing to simulate the propagation of light in the waveguides was developed to assist in the design of the taps. The etching characteristics of KOH and KOH / isopropyl alcohol mixtures were determined. Waveguides with five serial out-of-plane taps were fabricated and tested, and the results analyzed.

ACKNOWLEDGMENTS

This thesis could not have been produced without the help of many individuals and organizations. Firstly, I would like to thank my supervisor, Dr. Jim McMullin, for his support and assistance throughout this project.

I thank the Telecommunications Research Laboratories (TRLabs) for their financial support and the use of their research facilities. The fabrication facilities of the Alberta Microelectronics Centre (AMC) also played a key role in this project.

I would like to thank the following individuals for their assistance:

Dr. Jim Broughton of the AMC, for performing thin film depositions and assistance with the SEM.

Yan Loke, formerly of the AMC, for his instruction in anisotropic etching.

Tran Tran of the AMC for his instruction in photolithography.

Ken Westra of the AMC for helpful discussions.

Graham McKinnon of the AMC for help with the photomask design and for his coordination of AMC resources.

Dr. Barrie Keyworth of TRLabs, for providing the dispensed waveguide data, and for helpful advice.

Dino Corraza and Terrance Rosadiuk of TRLabs for their assistance with the polymer dispensing system and optical measurements.

Finally, I would like to thank my parents for their support and encouragement throughout the course of my education.

TABLE OF CONTENTS

Chapter 1 - Introduction.....	1
1.1 Hybrid Optoelectronic Integrated Circuits	1
1.2 Serial Optical Distribution	2
1.3 Micromachined Waveguide Taps.....	4
1.3.1 Silicon Micromachining Basics	
V-Grooves	4
1.3.2 Centre Taps.....	6
1.3.3 Sidewall Taps.....	7
1.3.4 Serial Out-of-Plane V-Groove Tapping	8
1.4 Dispensed polymer waveguides.....	9
1.4 Outline of Remainder of Thesis.....	9
Chapter 2 - Waveguide Simulation	11
2.1 Simulation Technique	11
2.2 Initial Ray Distribution	15
2.3 Simulation Results.....	18
2.3.1 Dispensed Polymer Waveguide with Serial Taps.....	18
2.3.2 V-Groove Waveguide with Taps.....	19
Chapter 3 - Fabrication of Serial Waveguide Taps.....	22
3.1 Wet Chemical Anisotropic Etching of Silicon.....	22
3.1.1 Etching Systems	22
3.1.2 Etching Mechanism	23
3.1.3 Masking Materials.....	24
3.2 Etch Rate Analysis.....	29
3.2.1 KOH Etch Rates.....	29
3.2.2 KOH with IPA Etch Rates.....	30
3.2.3 Etch Smoothness	32
3.3 Implications of Etch Rates on Tap Design.....	34
3.3.1 Centre Taps.....	34
3.3.2 Sidewall Taps.....	39
Chapter 4 - Fabrication and Testing of Tapped Waveguides.....	46
4.1 Fabrication of Waveguides	46
4.1.1 Etching.....	46
4.1.2 Metalization of Taps	47
4.1.3 Deposition of Core and cladding Layers.....	49
4.2 Waveguide Testing	51
Chapter 5 - Conclusions	58
5.1 Summary of Work.....	58
5.2 Recommendations for Future Work	59
References	60
Appendix A - Calculation of Angles of Reflected Rays	64
Appendix B - Simulation Software Details	67

Appendix C - Lithography Procedures	70
---	----

LIST OF FIGURES

Figure 1.1 - Hybrid optoelectronic integrated circuit.....	2
Figure 1.2 - Side cross-section of 3 serial out-of-plane taps in a waveguide.....	3
Figure 1.3 - Top view of in-plane 50% tap.....	4
Figure 1.4 - Etching of v-groove in silicon.....	5
Figure 1.5 - Waveguide with two centre taps and reflective end facet.....	6
Figure 1.6 - Waveguide with a single sidewall tap and reflective end facet.....	7
Figure 1.7 - Angles of ray reflected from {525} sidewall.....	8
Figure 1.8 - Cross-section of triple dispensed polymer core waveguide	9
Figure 2.1 - Sample waveguide power vs. distance plot	12
Figure 2.2 - Sample of tapped power vs. surface position graph.....	13
Figure 2.3 - Sample tapped power vs. distance simulation output.....	14
Figure 2.4 - Sample of cross-sectional power plot.....	15
Figure 2.5 - Comparison of beam radius for ideal and simulated Gaussian beams.....	16
Figure 2.6 - Comparison of peak power for ideal and simulated Gaussian beams.....	17
Figure 2.7 - Comparison of actual and simulated tapped power for dispensed waveguide	18
Figure 2.8 - Waveguide power vs. distance for balanced taps	20
Figure 2.9 - Cross-sectional power at increasing distances from tap.....	21
Figure 3.1 - Convex corner undercutting	25
Figure 3.2 - Results of partial etching of pattern of previous figure	25
Figure 3.3 - Top surface of mesa formed by various planes	27
Figure 3.4 - Diagonal etch distance.....	30
Figure 3.5 - KOH/IPA vertical etch rate.....	31
Figure 3.6 - KOH/IPA diagonal etch rate	32

Figure 3.7 - Cross-section and top view of wafer during processing	35
Figure 3.8 - Evolution of tap size as etching time increases	37
Figure 3.9 - SEM photo of partially etched centre tap.....	38
Figure 3.10 - SEM photo of finished centre tap.....	38
Figure 3.11 - Mask pattern for three sidewall taps.....	40
Figure 3.12 - Evolution of { 100 } silicon surface under mask.....	40
Figure 3.13 - Photo of partially etched sidewall tap	41
Figure 3.14 - SEM photo of sidewall tap.....	42
Figure 3.15 - Idealized sidewall tap.....	42
Figure 3.16 - Cross-section of idealized sidewall tap and waveguide	43
Figure 3.17 - Geometry for mask design.....	44
Figure 4.1 - Cross-section of waveguide with polymer lower cladding.....	48
Figure 4.2 - Cross-section of completed v-groove waveguide.....	50
Figure 4.3 - Cutback measurement results.....	52
Figure 4.4 - Tapped power results	53
Figure A.1 - Geometrical analysis of ray striking centre tap or end facet.....	64

LIST OF TABLES

Table 1.1 - Angles of various planes.....	7
Table 3.1 - Angle of incidence with upper surface for various tap planes.....	39
Table 3.2 - Mask Dimensions for 1:5 split	45
Table 4.1 - Comparison of measured tap powers and theoretical values.....	55
Table 4.2 - Comparison of loss measurements using decreased tap size model.....	56
Table A.1 - Angles of incidence of tapped rays on upper surface of waveguide.....	65

LIST OF ABBREVIATIONS

BOE	buffered oxide etch
CsOH	cesium hydroxide
CVD	chemical vapour deposition
EDP	ethylenediamine pyrocatechol
GaAs	gallium arsenide
HMDS	hexamethylene disilazane
IC	integrated circuits
IPA	isopropyl alcohol
KOH	potassium hydroxide
NH ₄ OH	ammonium hydroxide
OE	optoelectronic
OEIC	optoelectronic integrated circuit
RPM	revolutions per minute
SEM	scanning electron microscope
Si ₃ N ₄	silicon nitride
SiO ₂	silicon dioxide
TMAH	tetramethyl ammonia hydroxide

CHAPTER 1 - INTRODUCTION

1.1 HYBRID OPTOELECTRONIC INTEGRATED CIRCUITS

In the late 1960's, it was suggested that optical systems could be created using "integrated optics" [1]. This term describes the combination of several optical devices on a single substrate, interconnected by waveguides. It is analogous to the interconnection of electrical components on a single substrate in integrated electronics. This concept of integration was later extended by A. Yariv [2] to the concept of "optoelectronic integrated circuits" (OEICs). His idea was to integrate not just optical and optoelectronic components, such as lasers and photodetectors, but also conventional integrated electronic circuits such as laser drivers and amplifiers. III-V semiconductors such as GaAs could provide the transistors, lasers and detectors, all on a single substrate.

One of the primary advantages of OEICs is that they allow improved performance of optical semiconductor devices. As an example, one of the limits in the speed of a directly modulated laser is the parasitic inductance and capacitance introduced by the interconnection of the laser and driver chips and their packaging. Integrating these devices on a single substrate could significantly reduce these parasitics, hence increasing the maximum modulation rate[3]. It is also hoped that in the long run, fabrication costs will be lower, due to the smaller size and packaging of the devices [4].

Unfortunately, accompanying these advantages are some difficulties in achieving practical OEICs for today's marketplace. OEICs require very complex growth procedures, largely due to the difference in the requirements between optical and electronic devices. Many successive growth and etching stages are necessary. It is very difficult, if not impossible, to simultaneously optimize devices for high speed electronic, photonic, and waveguiding purposes on the same semiconductor substrate [4]. The performance in one area is likely to suffer at the expense of others. Other issues include the cost of large area wafers of III-V compounds like InP, and the manufacturing yield when fabricating such complex circuits [5]. Work is being done on OEICs on substrates other than III-V compounds. Silicon, while it lacks the direct bandgap required for creating lasers, can have III-V compounds grown on it in strained layers, a difficult process known as heteroepitaxy [6].

A solution to some of these problems can be found in the "hybrid" integration of optoelectronic circuits. Rather than trying to fabricate all the components on a single semiconductor wafer, components are fabricated in the most appropriate material, and then

combined together onto a single substrate. Figure 1.1, taken from [7], illustrates this technique. GaAs ICs are surface mounted on a glass substrate, which contains waveguides and a metalization layer for electrical interconnects. The maturing of flip-chip solder bonding technology [8] allows the very precise automated alignment of chips onto the "mother" substrate.

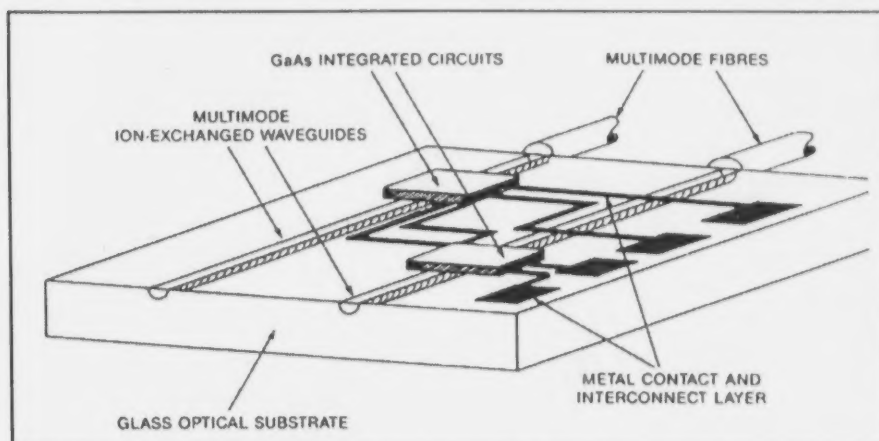


Figure 1.1 - Hybrid Optoelectronic Integrated Circuit

Hybrid integration allows the use of substrates other than III-V compounds. Glass and silicon are common choices, as they can be obtained in large sizes and are relatively inexpensive. If silicon is used as the substrate, highly mature silicon electrical devices can be integrated onto the mother board, reducing the amount of flip-chip bonding required. Silicon also can be micromachined, as will be discussed in later sections, allowing several interesting structures unavailable in other materials.

An important consideration in hybrid integration is the distribution of the optical signals between the surface mounted optoelectronic chips. This is particularly an issue if the same data is to be distributed amongst several devices, such as a synchronizing clock signal. This thesis will examine one technique to solve this problem, the serially tapped waveguide.

1.2 SERIAL OPTICAL DISTRIBUTION

One promising idea for the distribution of optical signals for hybrid integrated optoelectronics is the waveguide with serial out-of-plane taps. This structure consists of an integrated waveguide which has a series of reflective surfaces carefully placed in it such that each taps a portion of the guided light out of the plane of the waveguide. This tapped light

can then be received by photodetectors surface mounted on the waveguide's substrate. See figure 1.2 for a diagram of the structure.

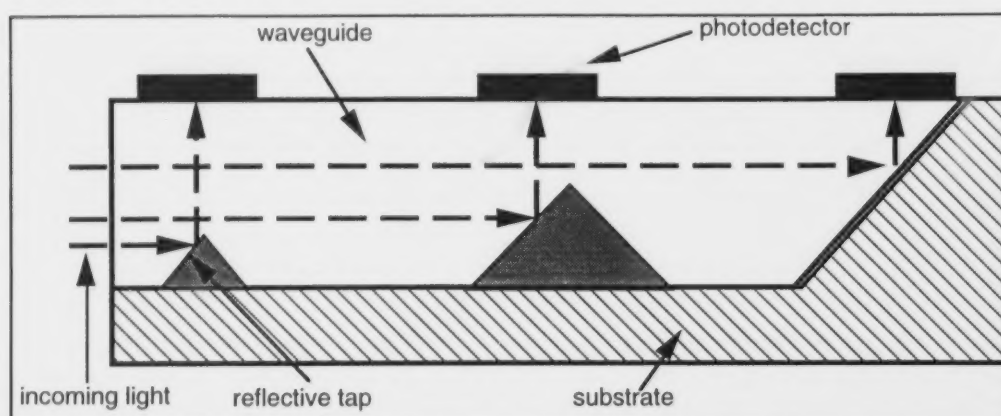


Figure 1.2 - Side cross-section of 3 serial out-of-plane taps in a waveguide

This type of structure offers many advantages for hybrid integration of optoelectronic circuits. The serially tapped guide uses much less real estate than a conventional y-junction waveguide splitter. The structure lends itself naturally to the implementation of an optoelectronic switching matrix [9]. To build a 10 x 10 OE switch, light from each of ten sources must be distributed equally to ten photodetectors. This could be accomplished through the use of ten parallel waveguides, each of which has ten out-of-plane taps. The first tap must remove 1/10 of the total light, the second 1/9 of the remaining light, and so on, until the last tap removes all the remaining light, one tenth of the original amount.

Some early work on out-of-plane tapping was done by Kokobun et. al [10], who suggested using the metalized end-facet of a v-groove waveguide as an out-of-plane reflector, which yields a single 100% tap. Some work has been done on serial in-plane tapping, deflecting a portion of the light in one waveguide into another lying at right angles [11][12]. Figure 1.3 illustrates this idea. By metalizing the end facets of the output guides, this in-plane technique could be converted to an out-of-plane tapping method.

The approach to serial out-of-plane tapping taken in this thesis deals with micromachining taps on the bottom[13] or sides [14] of v-groove waveguides. These taps will be described in detail in the following section.

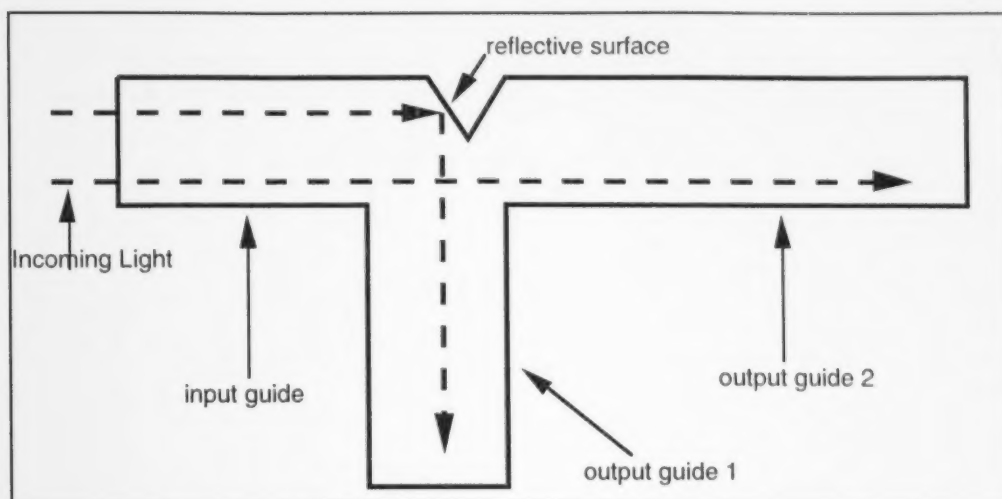


Figure 1.3 - Top view of in-plane 50% tap

1.3 MICROMACHINED WAVEGUIDE TAPS

1.3.1 SILICON MICROMACHINING BASICS: V-GROOVES

The two steps involved in the micromachining of silicon are photolithography and anisotropic etching. The photolithography steps result in a patterning of the silicon wafer, generating openings of a desired shape in a masking layer which expose the bare silicon beneath. The masking layer is chosen such that it is not significantly attacked by the anisotropic etchant. Anisotropic etching is etching which occurs more rapidly in some crystallographic directions than in others. Strong alkaline solutions, for example, tend to etch silicon much more slowly in the $\langle 111 \rangle$ directions than in other directions. Figure 1.4a shows a (100) silicon wafer with a rectangular opening in the masking layer aligned in the $\langle 110 \rangle$ direction. Figure 1.4b shows the etching having started, with the slow etching $\{111\}$ planes limiting the growth of the cavity at its ends and sides. The $\{100\}$ plane still defines the bottom of the opening. If the wafer is left in the solution, eventually the four $\{111\}$ planes will meet, and etching will effectively stop, assuming the rate in the $\langle 111 \rangle$ direction is very slow. A v-shaped groove will remain, bounded by $\{111\}$ planes (figure 1.4c). Provided the mask opening is properly aligned with the $\langle 110 \rangle$ direction, these $\{111\}$ sidewalls will be extremely smooth.

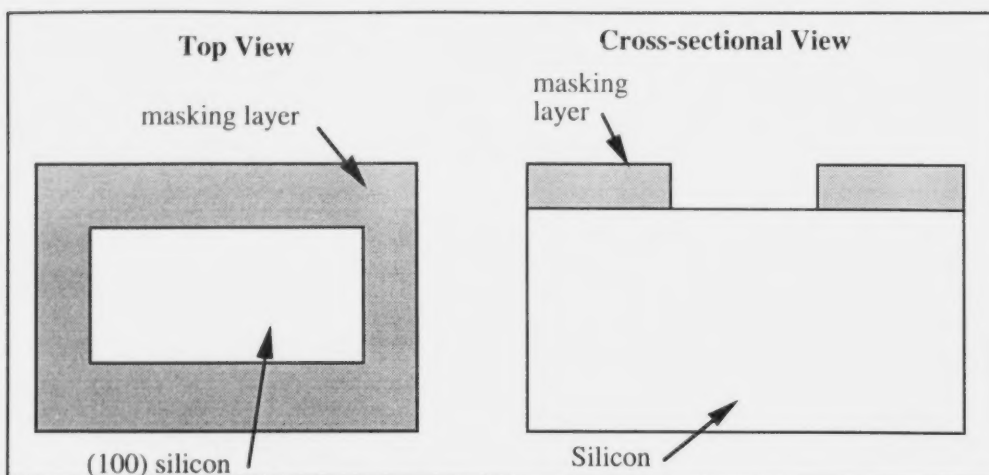


Figure 1.4a - Before etching

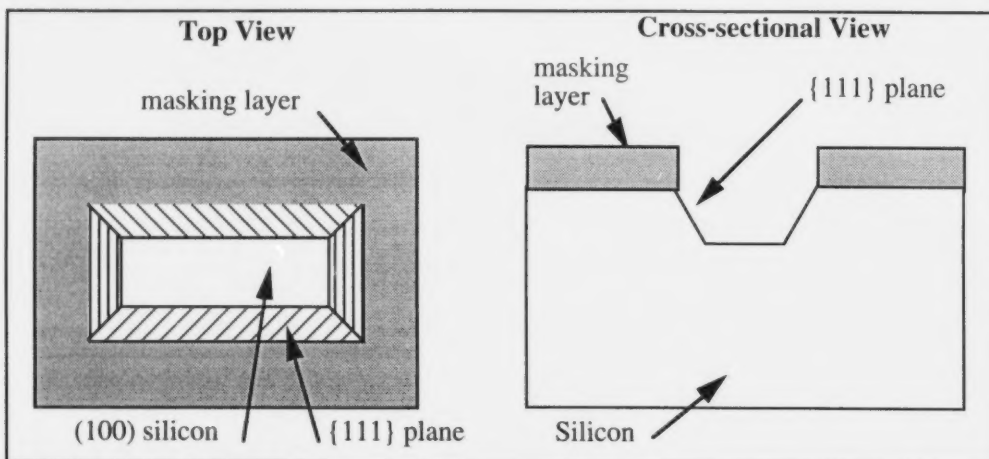


Figure 1.4b - Partially etched groove

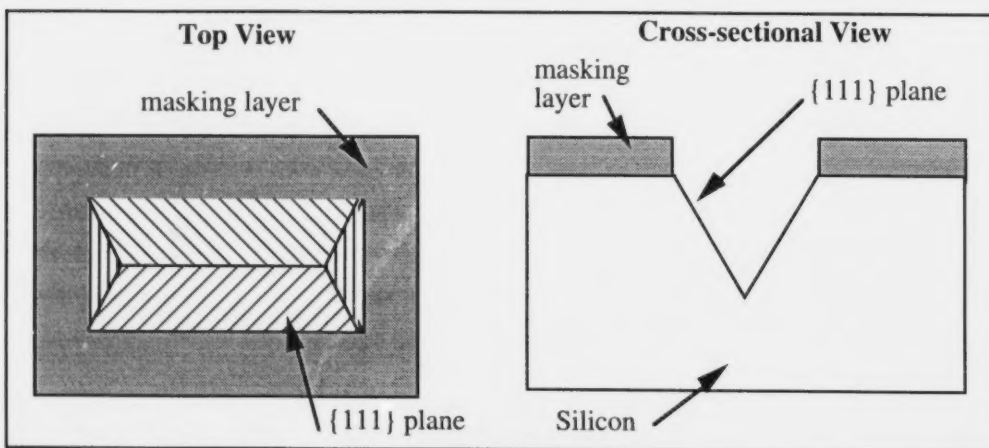


Figure 1.4c - Finished v-groove

Tsang et. al. [15] were the first to use this technique to generate optical waveguides. If the groove is coated with an oxide cladding layer and then filled with a higher index material, it can act as a waveguide. Because of the smooth single crystal sidewalls, the waveguide should have very low scattering losses. To couple light into these waveguides, larger v-grooves can be etched to hold and accurately position a conventional optical fiber, butted against the start of the v-groove guide [16]. The use of v-grooves to align optical fibers with waveguides and other integrated optical devices is now quite common (e.g.[17]).

1.3.2 CENTRE TAPS

The centre tap is so called because the reflective surface is centred horizontally at the bottom the v-groove waveguide. Figure 1.5 shows several views of a waveguide with a pair of centre taps, plus a reflective end facet.

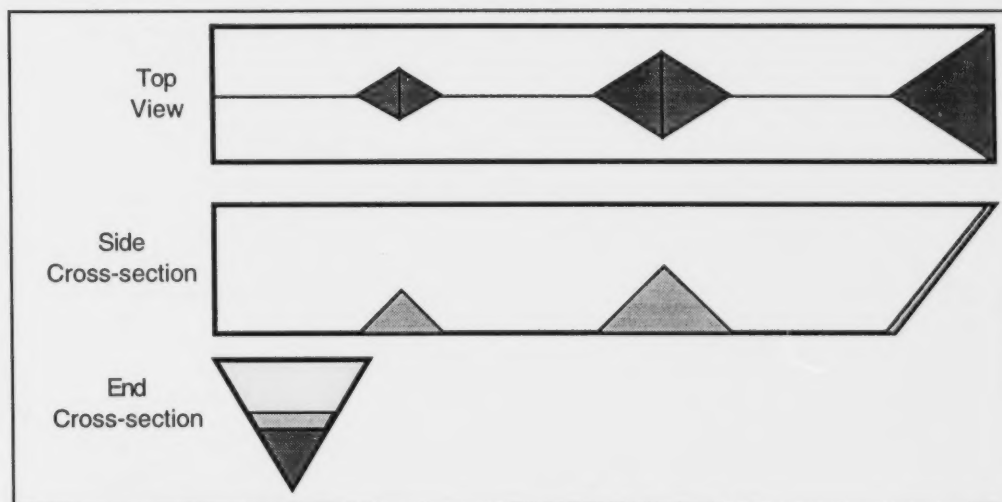


Figure 1.5 - Waveguide with two centre taps and reflective end facet

. By varying the size of each tap, the amount of light they extract can thus be controlled. The tapping planes must be at such an angle that light striking the surface of the tap will be reflected out of the guide. If the tap is at too shallow or steep an angle, the light will be internally reflected at the top surface of the waveguide, or will escape at such a small angle that a surface mounted photodetector will have difficulty capturing it. The angle of the tapping planes is determined by the crystal plane which forms the tap. Table 1.1 shows the angles various planes make with the surface of the silicon wafer.

Plane Type	Angle with Horizontal $\langle 110 \rangle$
$\{111\}$	54.7°
$\{112\}$	35.3°
$\{113\}$	25.2°
$\{114\}$	19.5°

Table 1.1 - Angles of Various Planes

Ideally, the centre taps should be formed by $\{111\}$ planes. Were this the case, the light from the taps would be reflected at an identical angle to that of the $\{111\}$ end facet of the waveguide, which forms the final tap of the waveguide.

1.3.3 SIDEWALL TAPS

Sidewall taps are so named because the reflecting surfaces of the taps lie on the sides of the v-groove. Figure 1.6 shows a top view and an end view of waveguide with a single sidewall tap, and a reflective end facet.

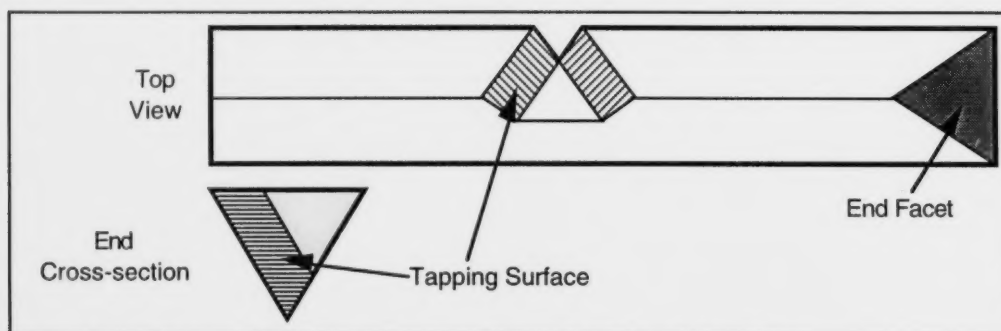


Figure 1.6 - Waveguide with a single sidewall tap and reflective end facet

A drawback of the sidewall tap is that the light reflected by the taps is traveling at a significantly different angle than that reflected by the end facet. A ray traveling straight down the guide striking the $\{111\}$ end facet will strike the top surface of the guide traveling backwards at an angle of 19.5° from the vertical. For a typical guide with a core refractive index of 1.56, this ray will exit into the air traveling backwards with an angle of 31° to the vertical, if no index matching is done between the guide and the detector. A ray traveling straight down the guide striking a sidewall tap formed by $\{525\}$ planes will continue to travel forward, making an angle of 76.6° degrees with the longitudinal axis of the guide when viewed from above, and 23° degrees with the vertical when looking down the

waveguide axis (see figure 1.7). These angles do not include any refraction at a waveguide/air interface.

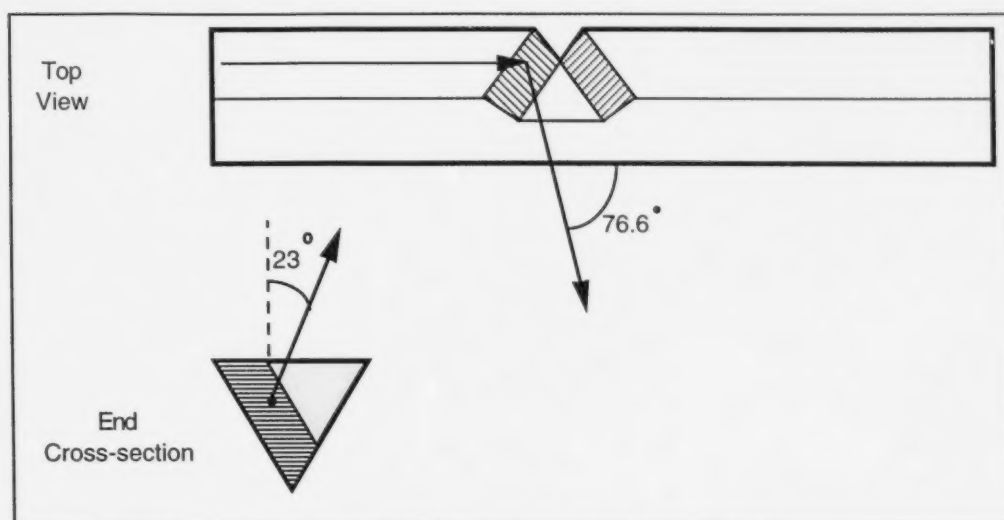


Figure 1.7 - Angles of ray reflected from {525} sidewall

If the tap is formed by {212} planes, the ray will be reflected at right angles to the waveguide longitudinal axis, and will make a 19.5 degree angle with the vertical when looking down the waveguide axis. Appendix A details the calculations of the reflected rays angles.

1.3.4 SERIAL OUT-OF-PLANE V-GROOVE TAPPING

The concept of the sidewall and centre taps in silicon v-grooves was developed at TRILabs in Edmonton, Alberta, by Dr. J. McMullin and students S. Kumar and E. Fei [13,14]. The original work was done using ethylenediamine pyrocatechol (EDP) to etch the v-grooves and taps.

The centre tapping surfaces were formed by {211} planes. Efforts to control the size of the taps encountered difficulties. More work needed to be done in this area.

The sidewall tapping surfaces were formed by {212} planes, although other extraneous planes were observed as well. Attempts were made to fabricate a balanced 12 x 12 tapping array, with 250 μm spacing between each tap. The results were unsatisfactory, there being differences among the power levels extracted by different taps.

It was decided to investigate further the concept of serial out-of-plane tapping using micromachined v-groove waveguides. More needed to be known about the effect of shadowing of downstream taps by upstream taps, and how to better control the tapping planes. A simulation program that could predict the performance of different waveguide

designs would permit optimization of various parameters. With these problems in mind, this thesis work was undertaken.

1.4 DISPENSED POLYMER WAVEGUIDES

Dispensed polymer waveguides are an active research area at TRILabs. The waveguides are created by using a syringe to dispense a UV curable optical adhesive onto a substrate, in the shape of the desired waveguide. The polymer is the same as that used for the core material for the v-groove waveguides discussed in this thesis. The surface tension in the liquid polymer causes it to have a curved upper surface, which can be modeled as an arc of a circle. As a single layer of polymer tends to be much wider than it is high, several dispensing passes are used, building up thicker and thicker layers. The radii of the circular cross-section grow smaller as the polymer is dispensed onto a curved surface rather than a flat substrate. Figure 1.8 shows a photograph of one of these waveguides, fabricated using 4 passes. The first pass dispenses a lower cladding layer, with a refractive index of 1.54. Three more passes dispense the core layer, which has index 1.56.

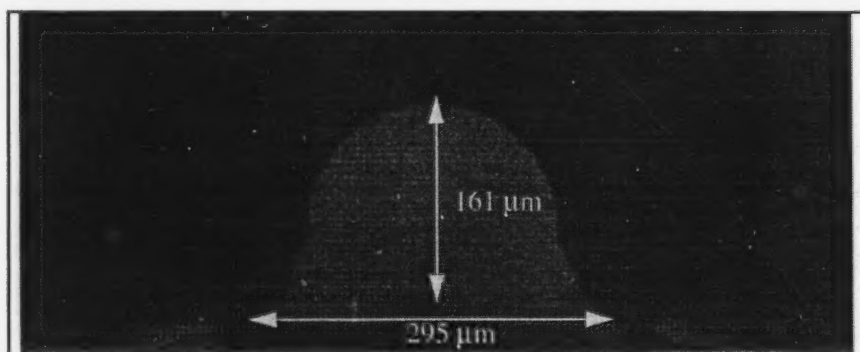


Figure 1.8 - Cross-section of triple dispensed core polymer waveguide

Taps can be made in these waveguides by carefully making an incision into the top surface of the waveguide with a very sharp blade, at a 45° angle. This creates a small air gap, which will reflect light out of the plane of the waveguide, much like a centre tap. By controlling the depth of the incision, the amount of tapped light can be controlled.

1.4 OUTLINE OF REMAINDER OF THESIS

Chapter 2 of this thesis discusses a computerized simulation of the propagation of light in multimoded waveguides with serial out-of-plane taps. Chapter 3 deals with the fabrication procedures for serially tapped v-groove waveguides. Chapter 4 gives the results

obtained when testing the guides. Chapter 5 consists of a discussion of the results obtained and recommendations for future work.

CHAPTER 2 - WAVEGUIDE SIMULATION

2.1 SIMULATION TECHNIQUE

In order to facilitate the design of the serially-tapped waveguides, a computerized simulation of the guides and taps was created. A simple ray-tracing technique was used to model the propagation of light in the guides. This technique assumes that geometrical optical principles account for all the relevant phenomena observed in the waveguide, that interference and diffraction do not play a significant role. As the dimensions of the multimode waveguides being investigated are many times larger than the wavelength of light used, this assumption should be valid.

A detailed description of the simulation programs may be found in Appendix A. A brief description will be given here. Each waveguide is modeled as a series of planes and curves, representing the boundaries of the core region of the guide. Each boundary is assigned an index of refraction, a complex one in the case of metalized taps. A large number of rays (one hundred thousand to several million) are launched at the input end of the guide, each with a unique combination of starting position and direction. Each ray is initially assigned an identical power value, and an electric field polarization. The distribution of rays is chosen to simulate the desired input beam shape. Section 2.2 gives more details on this aspect of the simulation. The rays are tracked individually as they travel in straight lines inside the core of the guide. Every time a ray strikes a boundary, the Fresnel reflection formulae are used to modify the ray power to account for any losses. When the ray power has been reduced below a given threshold, that ray is terminated, and calculations commence for the next ray. A propagation loss (in dB per cm) can be specified, reducing the ray power between bounces.

The program tracks several variables as the rays propagate. The total power inside the core of the guide is recorded as a function of distance. Figure 2.1 gives a typical plot of this data, for a v-groove waveguide with four centre taps and a reflective end facet. Power which is not reflected at a boundary is considered lost, with the exception of power transmitted through the top of the guide. This power is saved to a matrix based on its position in the guide. This allows the user to determine how much light is emerging from various locations on the surface of the guide. The angle at which this light exits the surface is not recorded. Figure 2.2 shows a plot of this matrix for a waveguide with 3 taps. The darker the spots on the graph, the more power is emerging. These transmitted power data can be summed across the width of the guide, if all that is desired is the amount of power tapped as a function of distance from the waveguide input. Knowing the total launched

power, this data can be used to determine the tapped power in dB, to compare it to power measured experimentally with a pickup fiber. Figure 2.3 show a typical plot of this type.

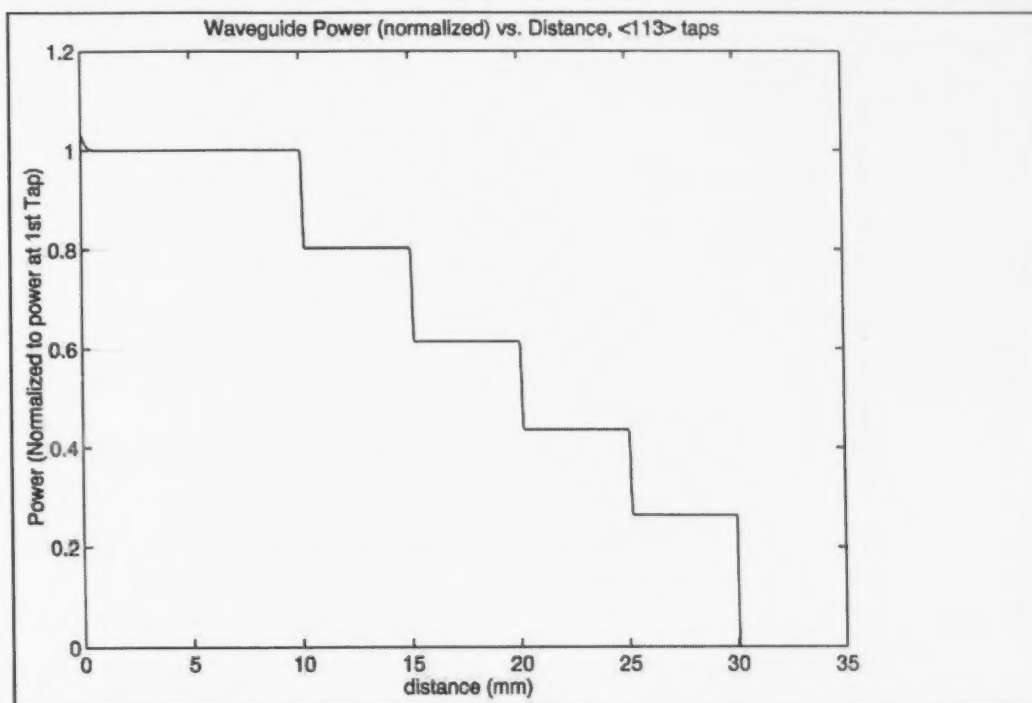


Figure 2.1 - Sample waveguide power vs. distance plot

A final analysis tool permits the determination of cross-sectional power. It is important to know how the power is distributed within the waveguide, to see how the light fills in between consecutive taps. This allows the determination of any possible shadowing effects. Tracking the power continuously in the cross-section of the guide would be far too computationally intensive, so a compromise is used. The user can specify various distances at which a power cross-section is desired. The program then inserts transparent planes at these points, divided up into a grid. The power of each ray striking a spot on this grid is added to the corresponding entry in a matrix. The ray is then allowed to continue propagating, with no change in its power or direction. Figure 2.4 show a two dimensional representation of a typical cross-sectional power matrix. The darker spots indicate greater intensity.

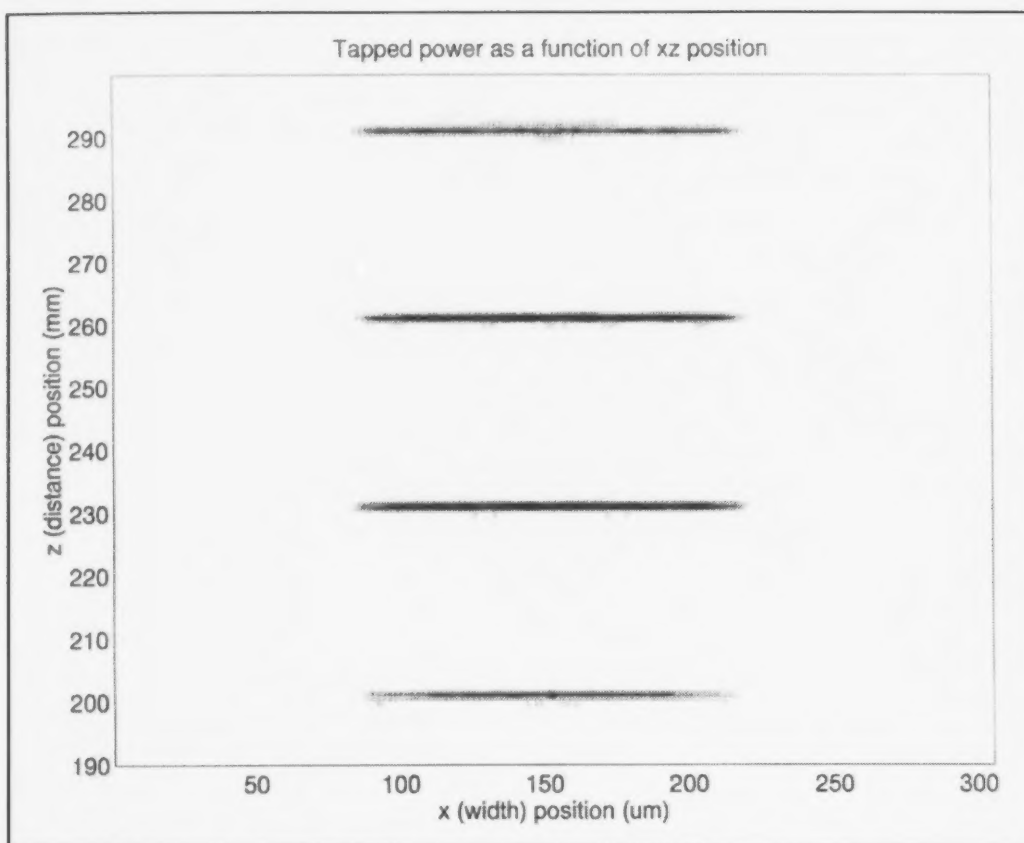


Figure 2.2 - Sample of tapped power vs. surface position graph

The program is easily adaptable to different waveguide geometries. Originally developed for analyzing v-groove waveguides, it was subsequently modified to take the curved top surface of the polymer core into account. Versions for simulating polymer waveguides with rectangular or circular cross-sections were later developed. Figure 2.4, showing a four pass dispensed polymer waveguide, demonstrates that quite complex geometries involving several intersecting circular cross-sections can be handled.

The program in its present form is designed to handle straight waveguides only. With fairly minor modifications, it could be changed to handle curved guides. The increased mathematical complexity of calculating the intersection of a ray with a three-dimensional curved surface would slow down the simulation speed.

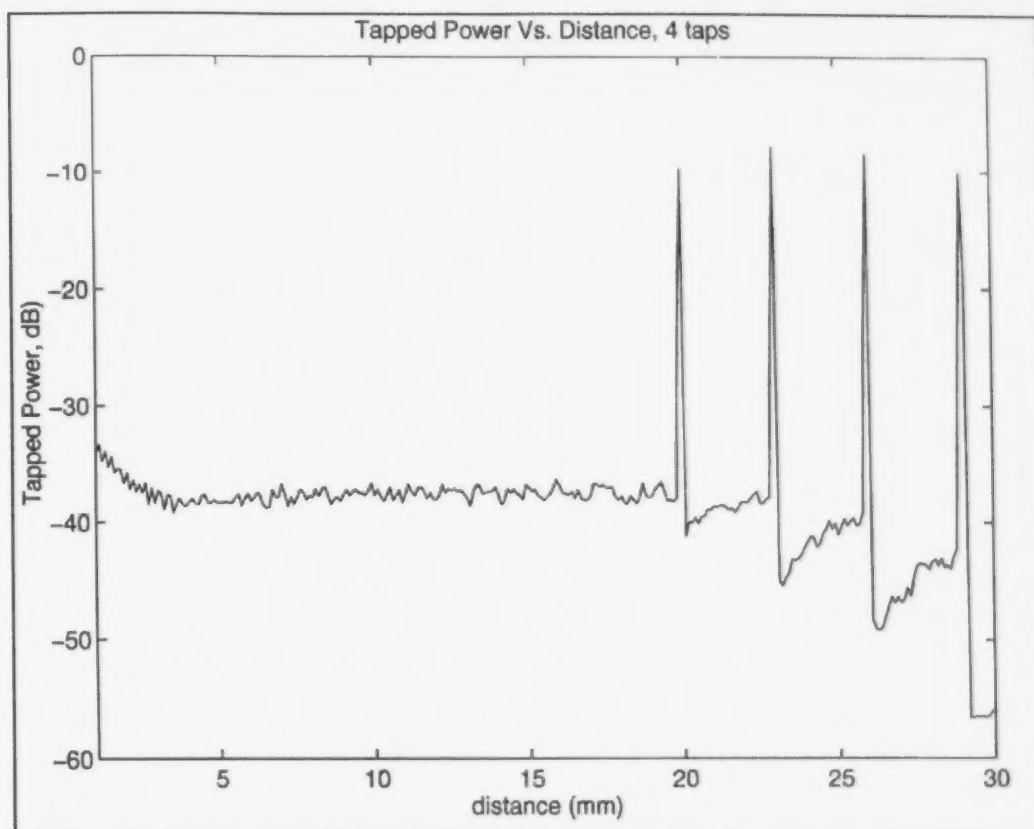


Figure 2.3 - Sample tapped power vs. distance simulation output

In its present form, to propagate 5.6 million rays through a 40 mm waveguide with four taps requires approximately 5 hours of computing time, on a DEC Alpha 3000 workstation. The number of rays used is dependent on the waveguide being tested and the input conditions, and is determined through a trial and error technique. Simulations are begun with a very large number of rays, and the number is reduced until changes are observed in the results. Typically, for multimode input simulation in v-groove waveguides, which mix the rays very well, a few hundred thousand were sufficient. Several million rays were used when single mode inputs to square waveguides were simulated, with a short distance to the first tap.

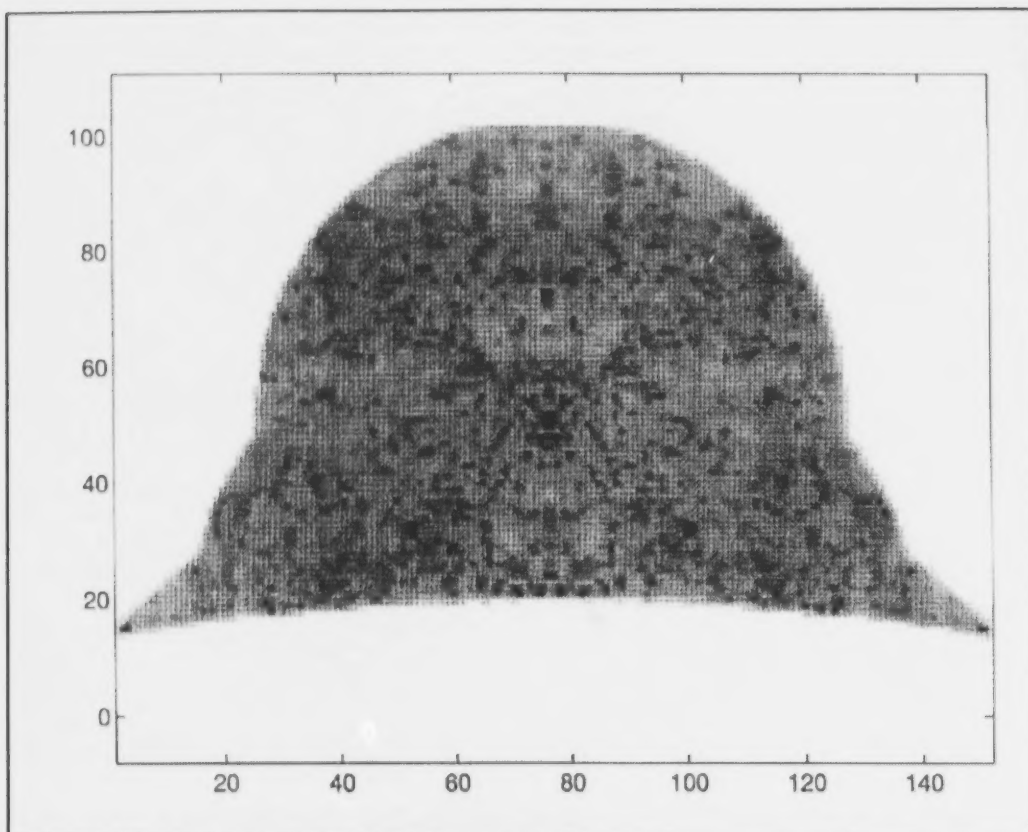


Figure 2.4 - Sample of cross-sectional power plot

2.2 INITIAL RAY DISTRIBUTION

The input conditions of the waveguide can be very important, particularly if a narrow diameter single mode fiber is being used to couple light into a guide which has a relatively short distance between the input facet and the first tap..

The output spatial power distribution of a single-mode fiber operating near cut-off is very nearly Gaussian [18]. An approximation must be used to simulate a Gaussian beam using a finite number of rays traveling in straight lines. It was decided to give each ray an equal amount of power, but have the angular and spatial distribution of the rays decrease in a Gaussian fashion from the centre of the beam. The parameters were chosen such that approximately $1/e^2$ of the power fell outside the desired beam radius, and $1/e^2$ of the rays were outside the beam divergence.

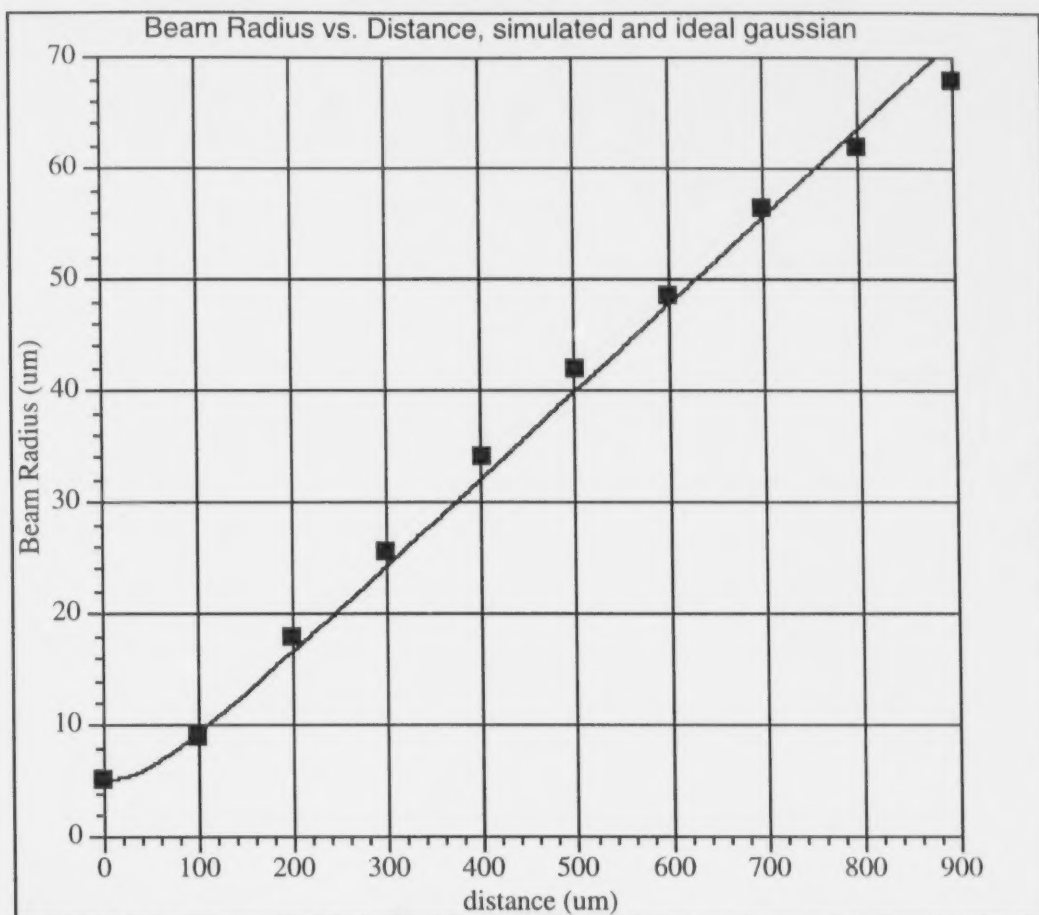


Figure 2.5 - Comparison of beam radius for ideal and simulated Gaussian beams

For an ideal Gaussian beam, with a Rayleigh range z_0 , and a peak intensity at the beam waist of I_0 , the peak intensity of the beam as a function of z is given as [19]:

$$I_p(z) = \frac{I_0}{1 + \left(\frac{z}{z_0}\right)^2}$$

The beam radius ($1/e^2$ power radius), for a waist beam radius of W_0 is given as:

$$W(z) = W_0 \cdot \left[1 + \left(\frac{z}{z_0}\right)^2 \right]^{\frac{1}{2}}$$

The beam radius and peak power of the simulated Gaussian beam was measured at 100 micron intervals for 900 μm of propagation in the waveguide, and compared to the behaviour of an ideal Gaussian beam with the same initial shape. These results are plotted

in figures 2.5 and 2.6. The solid points indicate the measured value of the simulated beam, and the line indicates the curve fit using the ideal Gaussian beam equations shown above. The beam radius matched quite closely. The peak power did not fall off as quickly as an ideal Gaussian should. This simulation used 5.6 million rays. Better matches to the ideal could be achieved using more rays, as the distribution of the rays could be made smoother.

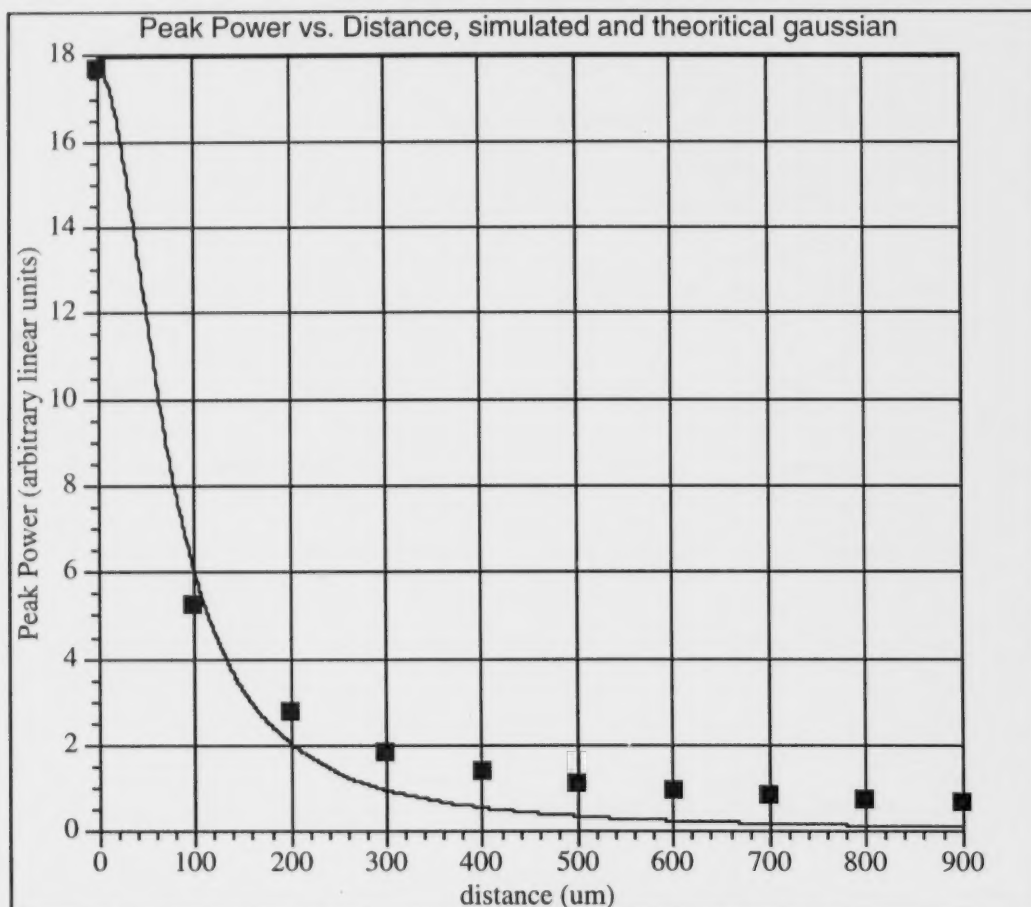


Figure 2.6 - Comparison of peak power for ideal and simulated Gaussian beams

When multimoded input fibers are used, it is assumed that the rays are uniformly distributed throughout the numerical aperture of the input guide. This technique has been used with success by other researchers [20].

2.3 SIMULATION RESULTS

2.3.1 DISPENSED POLYMER WAVEGUIDE WITH SERIAL TAPS

As the dispensed polymer waveguide tapping technology is more mature than the v-groove tapping technique, serially tapped polymer waveguides were used to verify the performance of the simulation program. A four tap waveguide fabricated by another research group was used as the test sample. The tapped power was measured by butt-coupling a single mode fiber to the waveguide, and using a 1 mm core pick-up fiber to measure the power exiting the top surface of the guide. The input fiber was positioned to maximize the power from tap 2. The taps were spaced 4 mm apart, with 20 mm between the input of the guide and the first tap. The waveguide propagation loss was 0.2 dB/cm. Using the measured tap sizes and spacing, this waveguide was simulated, and the simulated results were compared to the actual measured tap powers. Figure 2.8 shows this comparison.

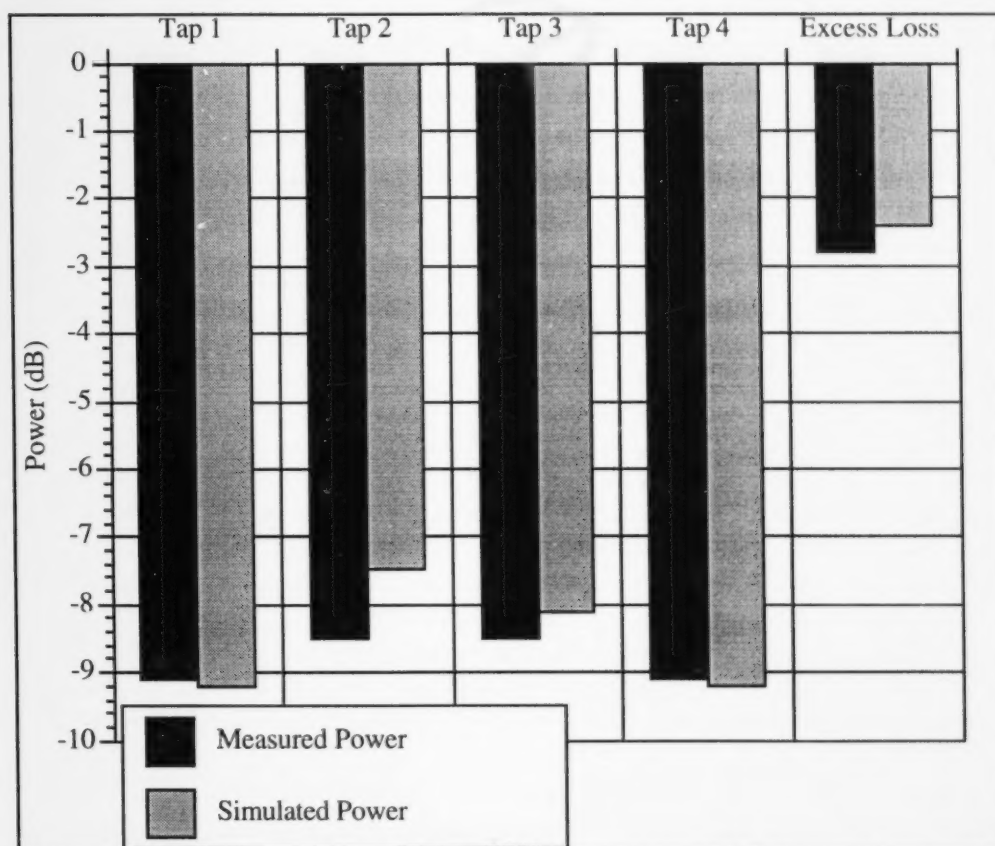


Figure 2.7 - Comparison of actual and simulated tapped power for dispensed waveguide

There was an excellent agreement between the measured power and the simulation results. There was a 1 dB difference between the powers for tap 2, but all other powers were less than 0.4 dB off. Changing the position of the input fiber in the simulation had less than a 0.5 dB effect on the balance of the powers. Differences between the measured and simulated values can be attributed to imperfections in the tapping surfaces, and variations in the depth of the cut when slicing the polymer. The small differences between measured and simulated values seen here would seem to indicate that the size of the dispensed taps can be controlled to a high degree of accuracy.

The core of this waveguide was approximately 170 by 200 microns, which is about twice the size of the v-groove guides being simulated. This test indicates that even when single mode fiber is used to couple light into the waveguide, the ray-tracing simulation gives quite good results.

2.3.2 V-GROOVE WAVEGUIDE WITH TAPS

The two fundamental parameters in the design of waveguide taps are tap size and tap spacing. The simulation results have shown that taps which are at a sufficiently steep angle will extract out any guided ray which hits them. If the power is uniformly distributed throughout the waveguide cross-section, the power tapped is proportional to the ratio between the cross-sectional tap area and the waveguide cross-sectional area. Figure 2.8 illustrates this, showing the total power in the waveguide for a five tap guide, with tap areas of 1/5, 1/4, 1/3, 1/2, and 100% of the waveguide cross-section. It yields a perfect 1:5 split, assuming that the propagation loss is minimal. These taps were spaced 5 mm apart.

If the taps are too close together, the rays will not have enough distance to redistribute themselves in the waveguide, and the taps will cast "shadows". Shadowing will result in a decrease in the tapped power at all taps after the first. This power will appear as extra power tapped by the end facet of the guide. This simulation program proved quite useful for investigating how quickly the light refills the guide after a tap, for different tap sizes and geometries. Figure 2.9 shows three-dimensional plots of the cross-sectional power in a v-groove guide, at 0.1 mm intervals. A 25% tap is located at 20.05 mm. The power is evenly distributed throughout the waveguide cross-section at 20.0 mm. After the tap, at 20.1 mm, the tap has removed all the power in the lower portion of the guide. At each subsequent cross-section, the power can be seen gradually filling into the lower half of the waveguide. Clearly after 0.5 mm, there is still an uneven distribution of the power.

After extensive simulation, it was concluded that in v-groove guides, tap spacings of 3 mm should be sufficient to avoid any shadowing effects. Tap spacings of less than 1 mm

showed significant degradation in their performance. Sidewall taps appear to be slightly less vulnerable to shadowing effects, likely due to their lack of symmetry.

When these simulation runs were completed, work commenced on fabricating centre and sidewall taps.

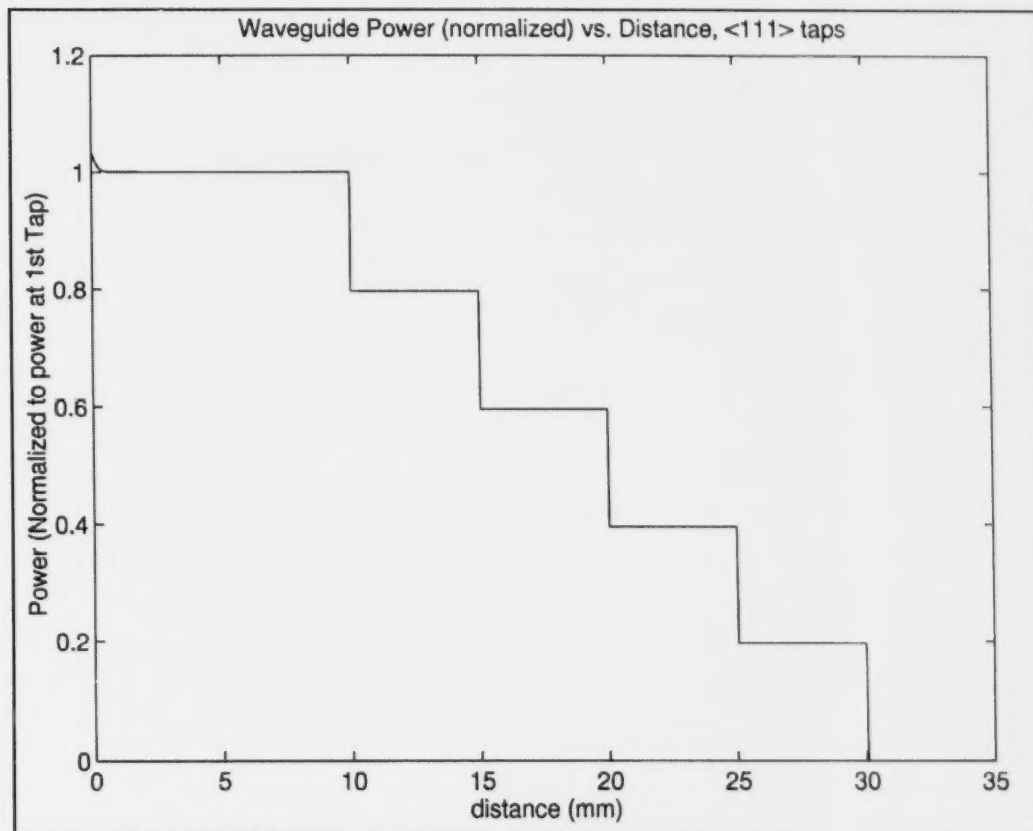


Figure 2.8 - Waveguide power vs. distance for balanced taps

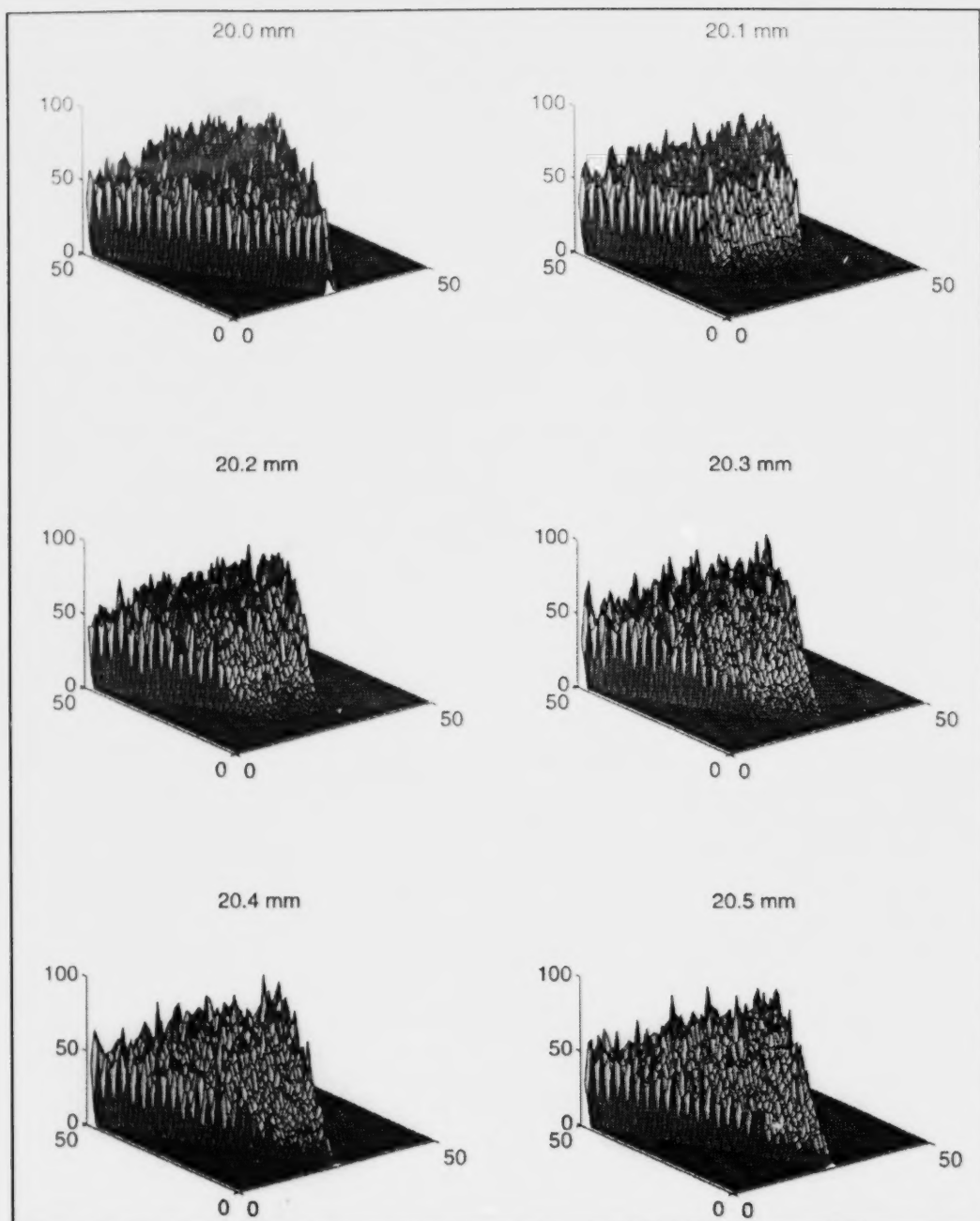


Figure 2.9 - Cross-sectional power at increasing distances from tap

CHAPTER 3 - FABRICATION OF SERIAL WAVEGUIDE TAPS

3.1 WET CHEMICAL ANISOTROPIC ETCHING OF SILICON

When single crystal silicon wafers are placed in certain alkaline solutions, some crystallographic directions are etched more quickly than others. Specifically, etching in the $\langle 111 \rangle$ direction is significantly slower than in the $\langle 100 \rangle$ or $\langle 110 \rangle$ directions. The relative etch rates are determined by the type of etchant, its concentration and temperature.

3.1.1 ETCHING SYSTEMS

The two most commonly used anisotropic etchants for silicon are aqueous potassium hydroxide (KOH) and an aqueous mixture of ethylenediamine and pyrocatechol (EDP) [21,22]. Among the less commonly used etchants are hydrazine, tetramethyl ammonia hydroxide (TMAH), cesium hydroxide (CsOH), and ammonium hydroxide (NH₄OH).

When choosing the etching system to be used for making serially tapped v-groove waveguides, several factors were considered, notably safety and etching characteristics.

Hydrazine was ruled out, as it is a very hazardous substance. The vapour is not only highly explosive, but is also carcinogenic. The etch rate also changes as the solution ages [23]. Little research is currently being done on etching with hydrazine.

NH₄OH yields very rough etch surfaces [24], which are inappropriate for waveguide applications. TMAH [25,26] yields better etched surfaces than NH₄OH, but the undercutting rate is significantly higher than for KOH [27]. Rapid undercutting rates make control of tap sizes more difficult, as will be shown in section 3.3.

CsOH has been used as an anisotropic etchant, yielding very smooth features [28], however there is little published data on its etching characteristics, particularly its undercutting rates. It was decided to use a solution about which more is known.

Previous work on serial out-of-plane taps in v-grooves have used EDP as the etchant. [13,14]. EDP does present some problems however. The solution is highly toxic, through both inhalation and absorption via the skin. Long term exposure to low levels of fumes can lead to bronchial asthma [29]. Also, when EDP is exposed to oxygen, it begins to discolour, and the etch rates increase significantly. To achieve predictable etch rates, it

was found that fresh solutions had to be prepared on a regular basis [30], increasing the user's exposure to the chemicals and creating a waste disposal problem.

KOH solutions, while highly corrosive, are much safer than EDP, and have a more consistent etching behaviour. Some investigators have added isopropyl alcohol (IPA) to KOH solutions, to alter the anisotropy [31,32]. It was decided that KOH would be the etchant of choice for this project.

3.1.2 ETCHING MECHANISM

The exact mechanism responsible for the anisotropy of etching in alkaline solutions is not well understood. It is now generally agreed [22,33] that the overall reaction is:



The silicate $\text{SiO}_2(\text{OH})_2^{--}$ dissolves into the etching solution, where it has been detected using spectrography [34], and the hydrogen gas can be observed bubbling up from the surface of the wafer. The current debate centres around why the {110} and {100} planes etch so much more quickly than the {111} plane.

One explanation was related to the fact that {111} silicon oxidizes more quickly than {110} and {100}, due to the differing available bond densities. It was theorized that a passivating oxide layer may form on {111} surfaces [35]. This oxide layer inhibits the etchant from reaching the underlying silicon. This passivation idea is also suggested in a more recent paper [36].

Another theory [22,33] suggests that as OH^- groups attach themselves to the dangling bonds of the surface silicon atoms, they withdraw charge, weakening the backbonds holding the Si atom in place. On the fast etching {100} surface, atoms have 2 dangling bonds per unit cell, while slow etching {111} surfaces have only one. Thus not only does the removal of an atom from the {100} surface require the breaking of fewer bonds than for {111}, but each of these bonds are weaker as well. The rapid etching {110} surface poses more of a problem for this theory, as like {111} surfaces it has only one dangling bond per atom. However, two of the three remaining bonds lie within the {110} surface, and may be more easily attacked than the more sheltered {111} backbonds [33].

Finally, others claim that the etching process must be looked at using the theories of crystal growth [37]. It is held that growth or etching takes place at "kink sites", where atoms have as many bonds to the crystal as they do to the surrounding liquid. The anisotropy of the etching is related to the number of available "kink sites" on a given

surface. On the {100} surface, every atom is a kink site. On the {111}, kink sites are created only by the removal of atoms, or through dislocations in the crystal structure. This theory doesn't seem to address the situation of {110} surfaces, however.

Very little is known about the role played by additives such as isopropyl alcohol. The IPA does not appear to participate chemically in the reaction [34]. It is suggested such additives serve only to vary the concentration of the etchant, to block the surface of the silicon from etchants, or allow the etched products to be removed more quickly [33].

3.1.3 MASKING MATERIALS

The two most commonly used masking materials for anisotropic etching are silicon dioxide (SiO_2) and silicon nitride (Si_3N_4). The two primary concerns when choosing a masking material are its resistance to the etchant, and the ease with which it can be deposited and patterned.

SiO_2 is very convenient to grow on silicon for thicknesses up to 1 micron, using thermal oxidation. The growth rate decays as the oxide layer deepens, making it difficult to grow thicker layers. It can also be deposited via chemical vapour deposition (CVD), but CVD oxide is not as etch resistant as thermal oxide [22]. EDP attacks SiO_2 at a fairly slow rate, about $8\text{\AA}$ per minute [21], or 1000 times slower than the rate in the $\langle 100 \rangle$ direction. Due to this slow oxide etch rate, care must be taken to remove any native oxide from the silicon surface before performing a timed etch. KOH solutions attack oxide more quickly, 20 to $60\text{\AA}$ per minute [21,35], or 100 to 300 times slower than the rate for $\langle 100 \rangle$ silicon. Patterning of SiO_2 is easily achieved using common photolithography techniques and buffered oxide etching (BOE). Appendix D describes the photolithographic steps.

If deep etching in KOH solutions is required, a CVD silicon nitride mask is usually used, as it is essentially not attacked at all. The etch rate is less than $8\text{\AA}$ per hour [38].

For the experiments performed here, using KOH with etch times less than 200 minutes, thermal SiO_2 was sufficient for masking purposes. Native oxide (typically $15\text{--}18\text{\AA}$ thick [39]) was not a concern, as it would be etched away within the first minute of exposure to the KOH.

3.1.4 CONVEX CORNER UNDERCUTTING

When an anisotropic etchant attacks a silicon surface bounded by a concave masking pattern (i.e. a simple rectangular opening), the etching at the edges of the opening

is limited by the slow etching $\{111\}$ planes, resulting in a v-shaped groove if etching is allowed to continue for a sufficiently long period of time. This was shown in figure 1.3. However, if the masking pattern has convex corners (see figure 3.1), a very different result is obtained. At these corners, fast etching planes are exposed, and the corner will be eaten away, undercutting the masking layer. Figure 3.2 shows a overhead view of the results obtained when the pattern given in Figure 3.1 is etched for a period of time. To show the undercut structure more clearly, the masking layer which would normally overhang the undercut areas is not shown in this drawing.

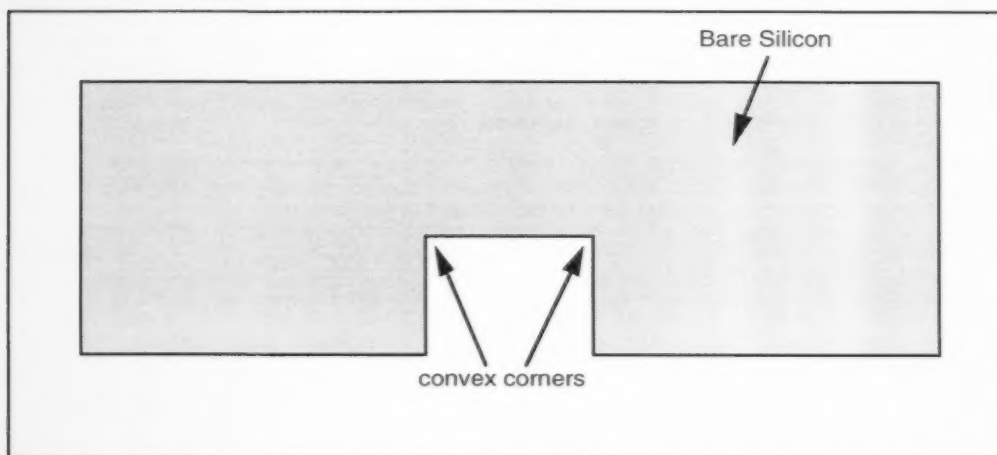


Figure 3.1 - Masking Pattern with Convex Corners

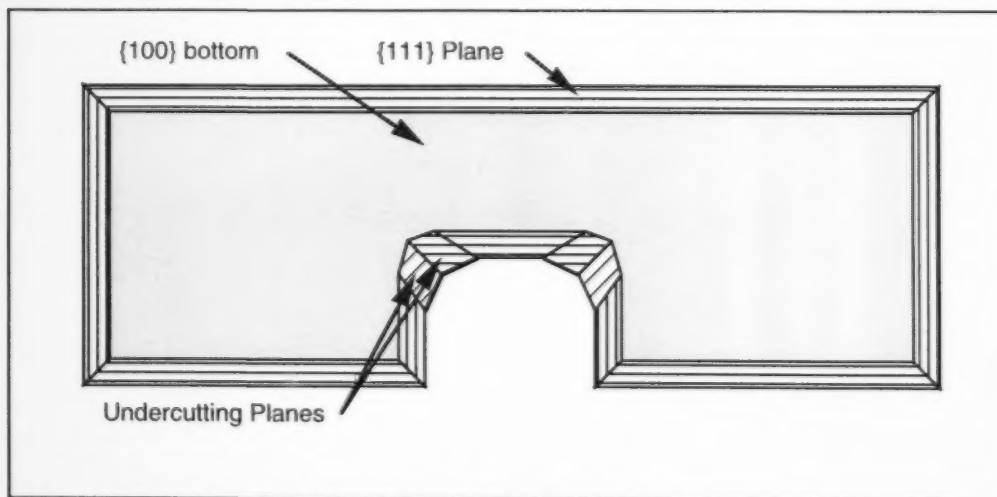


Figure 3.2 - Results of partial etching of pattern of previous figure

If this wafer were to be etched for a sufficiently long period of time, the convex portion of this pattern would be completely eaten away, leaving the familiar v-groove bounded on all sides by $\{111\}$ planes.

The planes which undercut these convex corners are determined by the etchant used. There is some confusion in the literature as to which planes are exposed by EDP, KOH, and KOH/IPA mixtures. The usual method used to determine which planes are present is to take SEM photographs of the undercut area, and measure the angles of intersection of the planes. Once these angles are known, the planes present may be calculated by comparing the measured intersection angles with the theoretical angles for various planes. Figure 3.3 shows the intersecting angles for the planes relevant to this thesis, when viewed from directly overhead. One possible source of confusion between {212} and {313} planes, as pointed out in [40], is the fact that a mesa formed by {212} planes is identical to one formed by {313} planes, rotated 45 degrees.

Most authors agree that when EDP is used, the undercutting planes are from the {212} family [14,40,41]. Bean alone claims that {313} planes are responsible [21]. Bao [42] mentions that others have found {211} planes, but does not give any references, and this may have been a typographical mistake.

For KOH and KOH/IPA, the situation is more diverse. Suggested undercutting planes for KOH are {212} [43], {31?} [44], {311} [45], and {411} [42,46,47]. In the experiments performed for this thesis, {411} planes were the only ones observed for etching in pure KOH. For KOH/IPA, the undercutting planes were said to be {212} by [40, 44] and {313} by Bean [21]. The KOH/IPA undercutting will be discussed in greater detail in section 3.2.2.

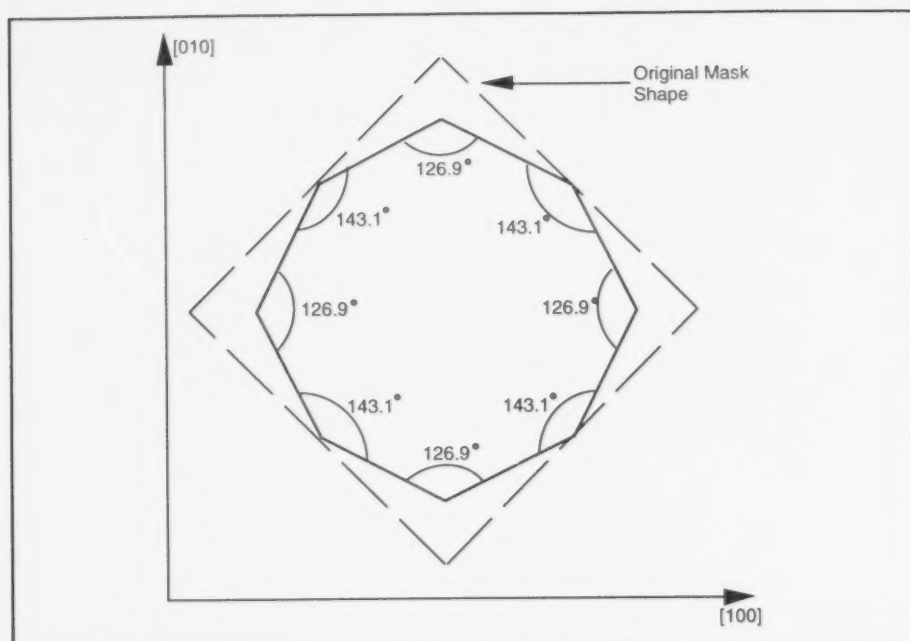


Figure 3.3a - Top surface of mesa formed by {212} planes

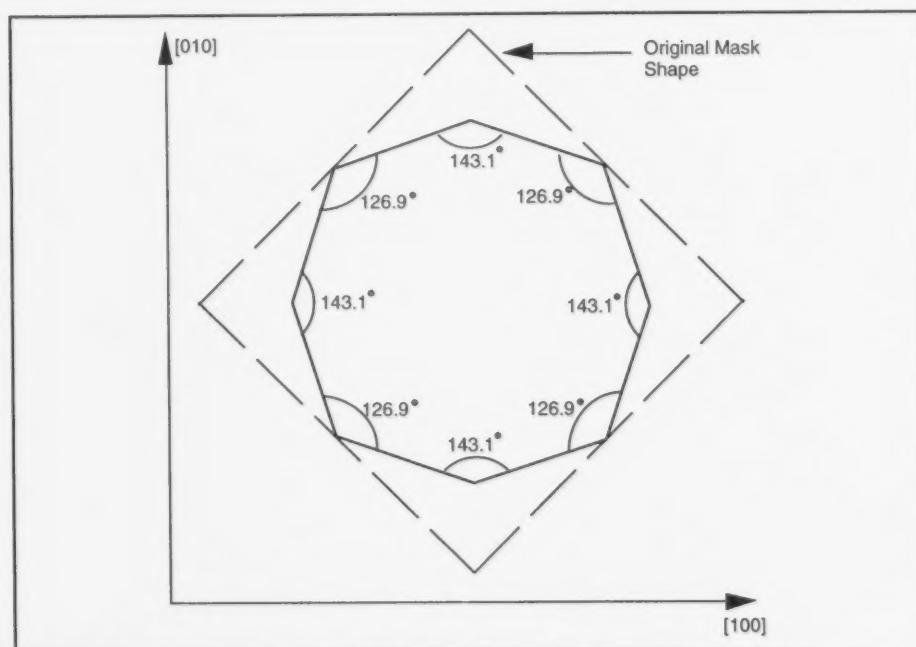


Figure 3.3b - Top surface of mesa formed by {313} planes

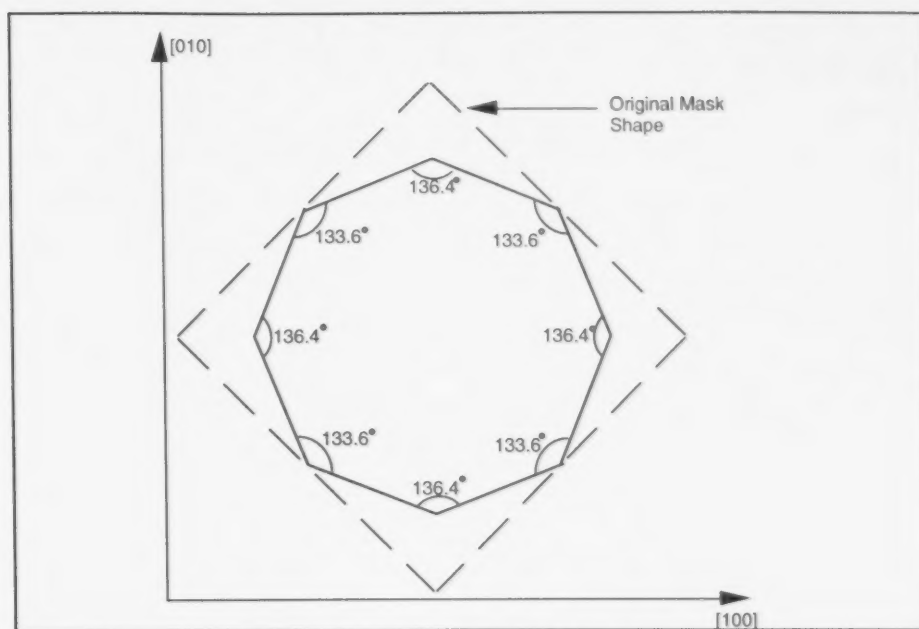


Figure 3.3c - Top surface of mesa formed by $\{525\}$ planes

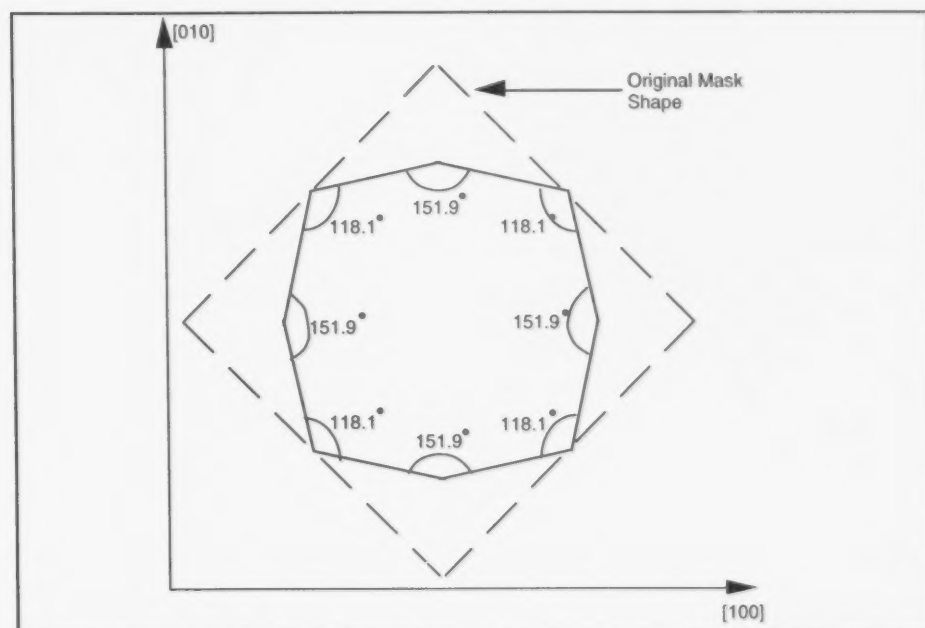


Figure 3.3d - Top surface of mesa formed by $\{411\}$ planes

3.2 ETCH RATE ANALYSIS

To characterize the etch rates of the KOH solutions being considered, a series of timed etches were performed. Numerous wafers were patterned photolithographically to yield many rectangular openings, with lengths of several centimeters and widths of 125 and 150 microns. Several rectangular stubs of masking oxide, similar to the one shown in figure 3.1, projected into the openings, to present convex corners to the etchant. The width of the stubs used were 75, 100 and 125 microns, and the lengths between 20 and 95 (in 25 μm steps). Also used in the timed etches were patterns with T-shaped openings, which again present a pair of convex corners to be etched. The patterned wafers were placed in a quartz container filled with the etchant. The container was covered with a water-cooled condenser cover to minimize the loss of vapour when the lid is removed. The containers were heated in an oil bath, with the temperature automatically controlled. Vigorous magnetic stirring was used prior to the immersion of the wafers to ensure an even concentration and temperature throughout the solution. For the first round of experiments, stirring was not used while the wafers were in the solution as there was no mechanism to prevent the stir bar from contacting the wafers sitting in the container. Lack of stirring was not deemed to be too much of a problem, as the wafers were being removed for analysis at fifteen to twenty minute intervals, after which the solution would be re-stirred. For the actual waveguide fabrication, longer etch times were necessary. For these experiments a larger etching container was used and a wafer holder elevated the wafers from the bottom of the container, allowing magnetic stirring to continue throughout the process. The following sections discuss the results obtained from these etch rate tests.

3.2.1 KOH ETCH RATES

A 30% wt. concentration of KOH was chosen for etching as this was reported to yield the smoothest planes [26]. The temperature was set at 78°C. A vertical (i.e. $\langle 100 \rangle$) etch rate of approximately 0.8 microns per minute was observed. This is somewhat lower than the 1.1 to 1.3 $\mu\text{m}/\text{min}$. reported by some authors [31,32] for 80°C. The undercutting rate was very rapid, with the corners receding along the diagonal (length "ld" in figure 3.4) approximately 1.4 $\mu\text{m}/\text{min}$.

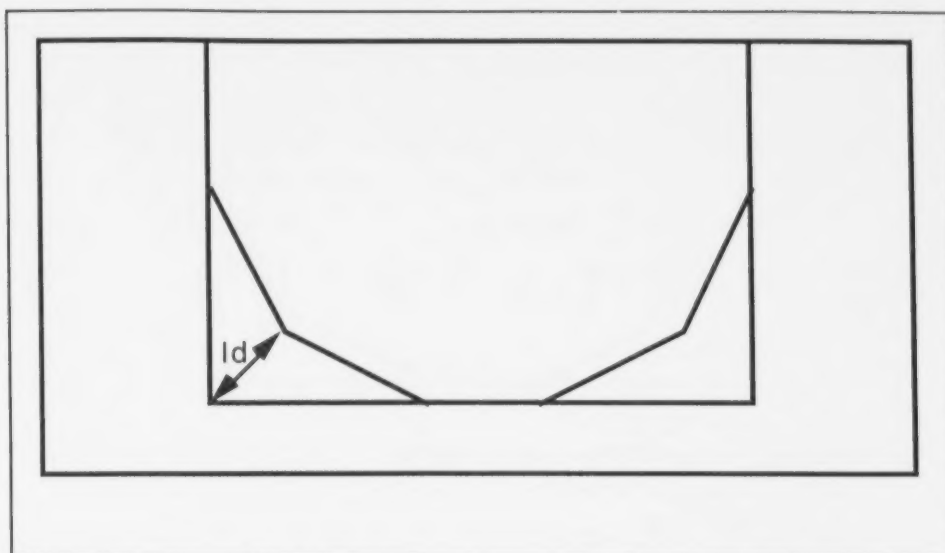


Figure 3.4 - Diagonal etch distance

The angle formed between the two undercutting planes, when viewed from directly above, was measured as being between 150° and 153° . This fits very closely with the 151.9° angle formed by two $\{41n\}$ planes. The planes were much too steep to be $\{414\}$, and were most likely $\{411\}$, in agreement with the results of most others. A 60°C etch was tried, but the diagonal rate was still larger than the downward rate, and the planes did not change.

3.2.2 KOH WITH IPA ETCH RATES

When IPA was added to saturate a 30% KOH solution, the etch rates changed dramatically. Approximately 250ml of IPA was added per litre of KOH solution. After stirring, this yields a two-phase solution, with a saturated KOH/IPA mixture on the bottom, and a layer of IPA (with some KOH) floating on top. The boiling point of IPA is 82°C [48], and the temperature of the oil bath used to heat the solution may vary slightly, so to ensure that the IPA is not rapidly boiled away, an etching temperature of 76°C was used. More IPA was added to the solution as the surface layer evaporated, ensuring that the KOH solution was always IPA saturated.

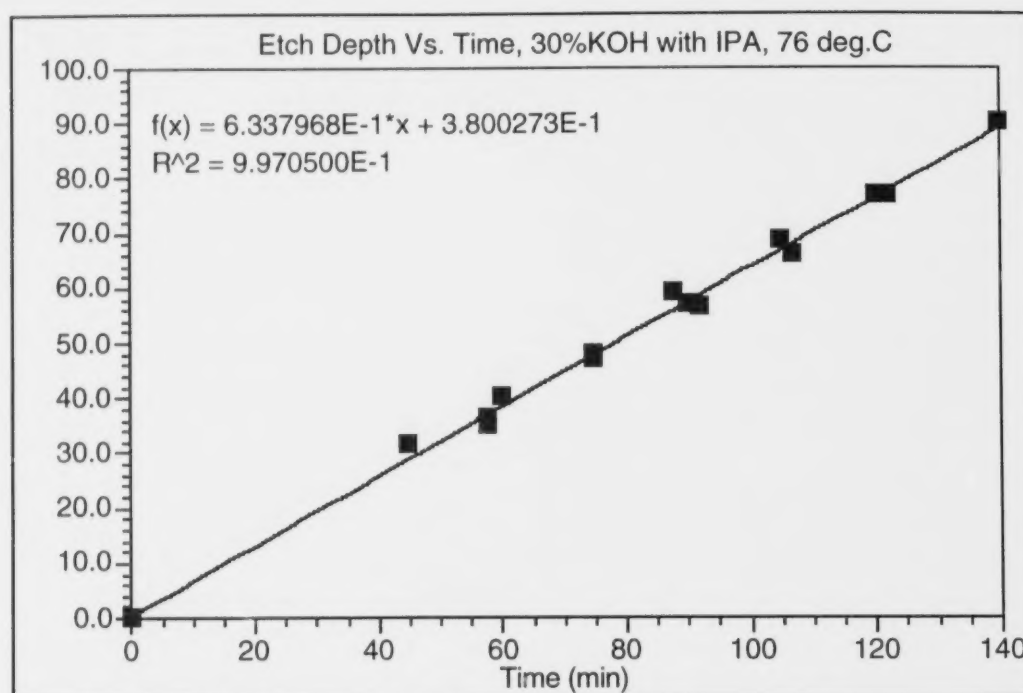


Figure 3.5 - KOH/IPA Vertical Etch Rate

Figure 3.5 shows a graph of etched depth vs. time. A linear curve fit indicates that the downward etch rate decreased slightly when compared to that obtained with pure KOH, to 0.63 $\mu\text{m}/\text{min}$. This graph also shows the consistency of the etch rate, as all the data points were taken over a period of two weeks. This decrease in the vertical etch rate when IPA is added is consistent with the observations of Price [31]

Figure 3.6 shows the diagonal etch distance ("ld" on figure 3.4), as a function of time. The data are a bit more variable, but some of this may be attributed to the 2 micron uncertainty in the length measurements, made using an optical microscope. Misalignment of the mask is another source of error in this measurement. The linear fit to the data gives a diagonal etch rate of approximately 0.31 $\mu\text{m}/\text{hr}$. This is significantly slower than that seen with pure KOH.

The angles measured between the adjacent undercutting planes at the convex corners were approximately 137° . The slope of the plane was measured as unity. This would identify the plane as a {525} plane, intermediate between a {212} and a {313}. Theoretically, {525} undercutting planes would meet at an angle of 136.4° , and have a slope of 1.08, so these are a very close match. While no other authors have reported {525} undercutting planes in KOH/IPA mixtures, the 131° angles measured by Puers and Sansen,

in [44], which they attributed to {212} planes, were intermediate between those expected for {212} planes and those expected for {525} planes.

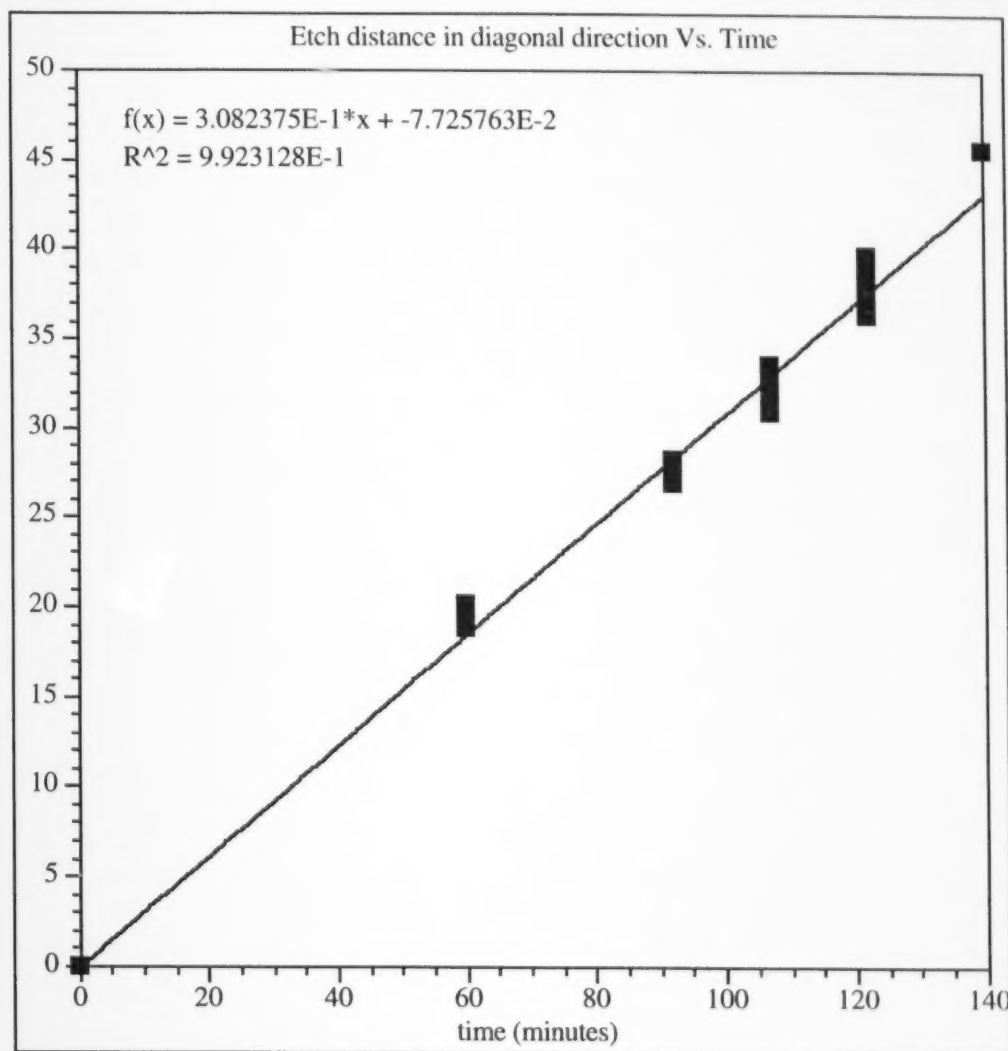


Figure 3.6 - KOH/IPA diagonal etch rate

3.2.3 ETCH SMOOTHNESS

A key requirement for micromachined waveguides is sidewall smoothness. Any irregularities will increase the scattering losses of the guides. While etching should ideally reveal perfect crystal planes, small silicon bumps, or "micro-pyramids" tend to appear on the silicon surfaces in some situations. Stirring the solution during etching greatly reduces the surface roughness, by an order of magnitude in one study [49]. It has also been observed that the roughness decreases with increasing KOH concentration. The temperature effects are less clear-cut. Findler [26] found that at 30% KOH concentration

higher temperature (60°C to 80°C) led to greater smoothness, while at 45% concentration, there was little difference. Tan et. al. [49] found that increased temperature increased the density of the hillocks, although no mention is made of their size. Others [43,50] found that increased temperature decreased the roughness.

Several investigators have examined the conditions contributing to the formation of the pyramids, with different hypotheses on their origin. Some attribute the pyramids to hydrogen bubbles clinging to the silicon surface[50]. The bubbles prevent the etchant from attacking the underlying silicon, acting as miniature masks as the surrounding silicon is etched away. Stirring the solution causes the bubbles to detach more rapidly from the surface, decreasing the roughness. The increase in smoothness observed when the solution was heated was attributed to the increased convection stirring.

Others blame SiO₂ impurities in the wafers, creating etch-resistant spots in the same manner as the hydrogen bubbles [43]. These SiO₂ impurities are formed when the wafer is heated to grow the thermal oxide needed for the masking layer. The roughness should decrease if the conditions were changed to increase the SiO₂ etch rate, i.e. increasing the temperature and concentration.

One phenomenon not mentioned in the literature is the effect of the age of the etching solution on the smoothness. Fresh mixtures of KOH, with or without IPA, were observed to yield much rougher surfaces than solutions which had been used for several days. If a solution has too much silicon dissolved in it, a residue can begin to form on the etched surfaces, formed by silicates which have polymerized [51]. This residue will lead to very poor etched surfaces.

Adding IPA to KOH mixtures increases the surface roughness, all other things being equal [52]. This coincides with the general observations made during the etch testing. Some experimenters [52] have tried adding a surfactant to reduce the surface tension of the solution, in an effort to improve etch quality. It was found that improvement was shown at lower KOH concentrations, when surfaces would normally be very rough. However, at concentrations of 25% and higher, which normally lead to fairly smooth surfaces, there was no noticeable improvement when the surfactant was added.

From this discussion, it may be concluded that for optimum smoothness, the solution should have some silicon dissolved in it, be magnetically stirred, and at as high a concentration as the etch rate constraints allow.

3.3 IMPLICATIONS OF ETCH RATES ON TAP DESIGN

3.3.1 CENTRE TAPS

Previously, centre taps have been fabricated using a two-stage masking procedure [13]. The basic idea is to generate a masking pattern with a thick layer of SiO_2 around the waveguide, and a thinner layer of oxide at each tap location. The steps used to achieve this structure are listed below. Figure 3.7 illustrates this process for making a single tap in the middle of a waveguide. Note that it is not to scale.

- 1 - Grow 0.6 microns of thermal oxide on wafer
- 2 - Use photolithography to make opening in photoresist in shape of waveguides, as shown in figure 3.7a.
- 3 - Use BOE to etch through the oxide in this region.
- 4 - Remove photoresist and grow another 0.3 microns of oxide on Si.
- 5 - Using mask similar to step 2, but with no openings in the regions where the taps are to be located, pattern photoresist as shown in figure 3.7b.
- 6 - Use BOE to remove exposed oxide (figure 3.7c).

Once this structure is achieved, the wafer is etched anisotropically, for a sufficiently long period that complete v-grooves will form in the unmasked areas. Next, a final BOE etch is performed, removing the oxide layer protecting the taps (figure 3.7d). As the oxide is thicker in the areas around the guide than it was over the taps, this oxide will remain after the tap oxide is gone. Finally, the wafers are anisotropically etched once again. The main v-grooves are already protected by the very slow etching $\{111\}$ planes, but the tapping areas are exposed to attack from above. Fast etching $\{mmn\}$ planes (where $n > m$) will eat their way down through the silicon separating the v-grooves. Eventually the $\{111\}$ planes will completely disappear, leaving the front $\{mmn\}$ plane as the tapping surface.

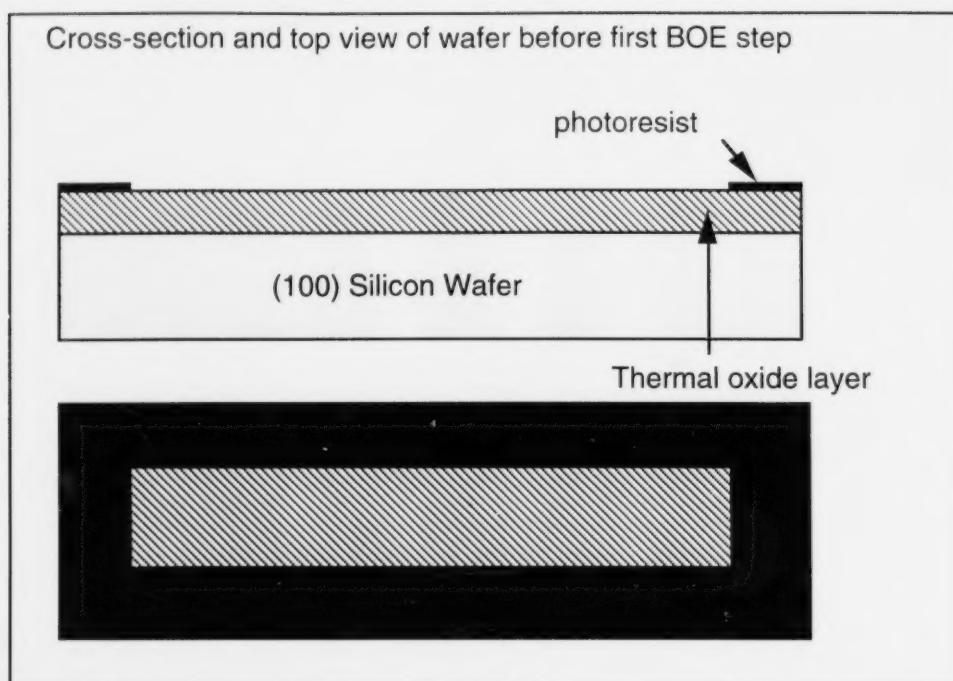


Figure 3.7a - Cross-section and top view of wafer before 1st BOE step

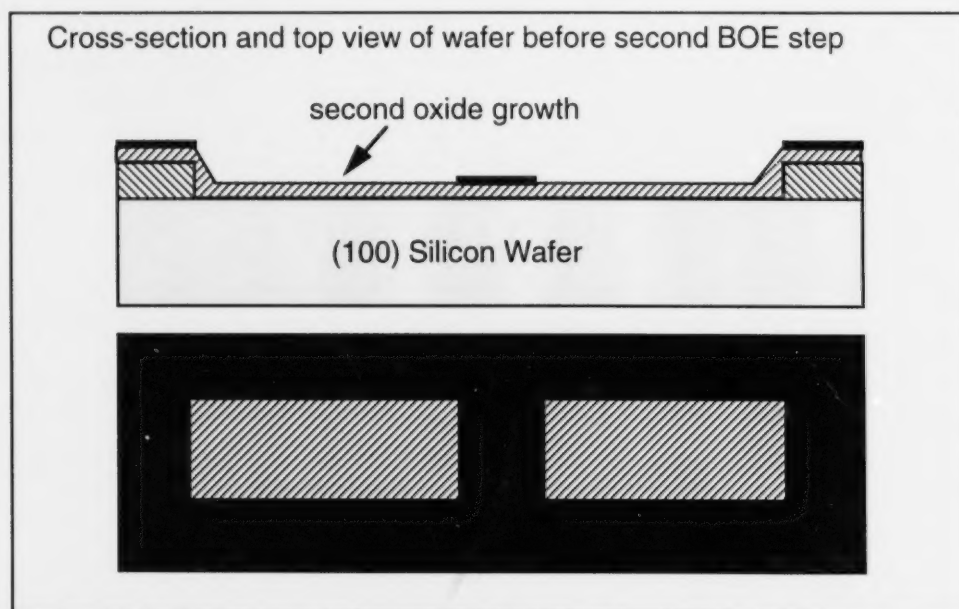


Figure 3.7b - Cross-section and top view of wafer before second BOE step

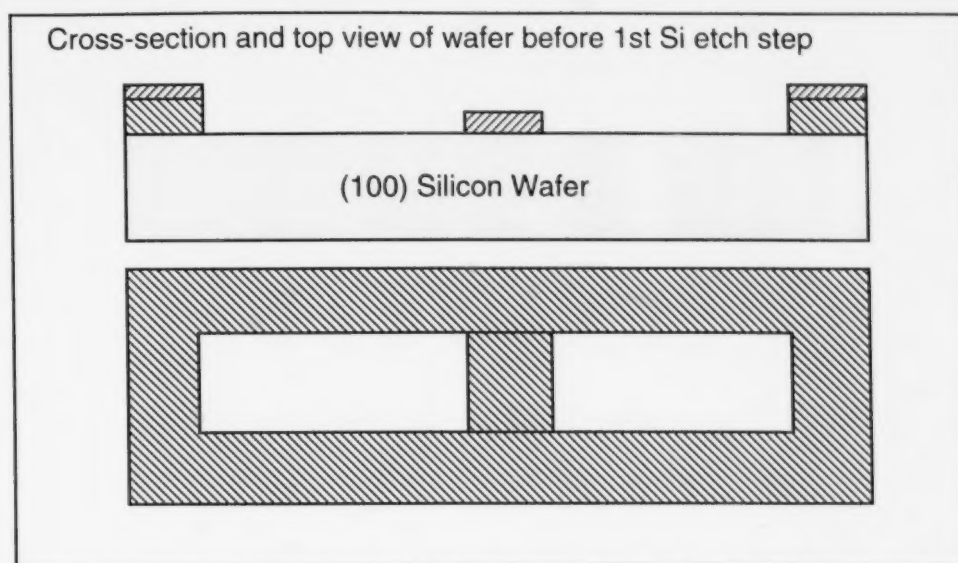


Figure 3.7c - Cross-section and top view of wafer before 1st Si etch step

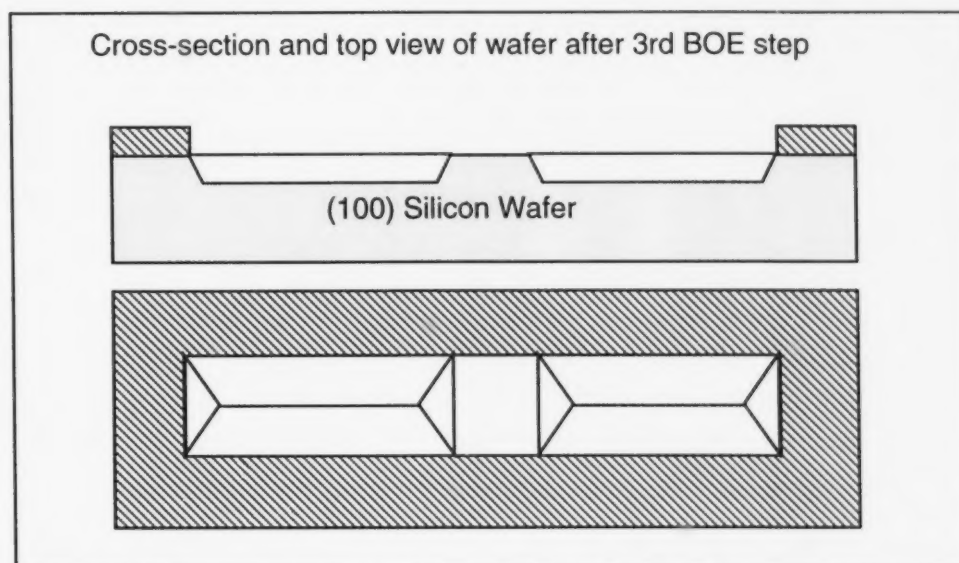


Figure 3.7d - Cross-section and top view of wafer after 3rd BOE step

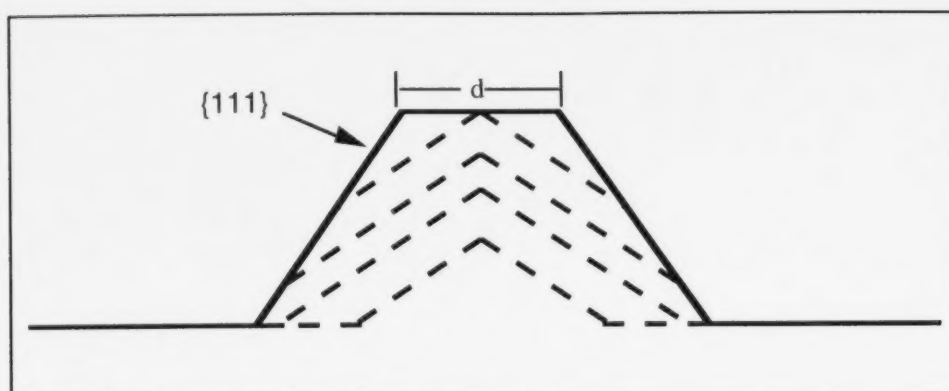


Figure 3.8 - Evolution of tap size as etching time increases

Figure 3.8 gives an example of the etch progression leading to the formation of the tap, showing the side cross-section. The longer the etch time, the smaller the tap becomes. By using the masking pattern to control the distance d shown in figure 3.8, and knowing the etch rate of the plane forming the taps, it should be possible to control the height, and hence the cross-sectional area, of the tap. The simulations discussed in Chapter 2 indicated that the ratio of power tapped to total waveguide power should be approximately equal to the ratio of the cross-sectional area of the tap to that of the guide. By placing several "humps" along the waveguide, with increasing length d , a serially tapped waveguide can be created. Several test etches were performed on wafers with 125 micron wide waveguide, with several taps per guide, the distance " d " varying between 55 and 120 microns. KOH and KOH/IPA were used as etchants. Most testing was done with a 30% KOH concentration, although 25% and 40% solutions were also used. Temperatures between 60 degrees and 80 degrees were tried.

Figure 3.9 shows a SEM photo of a partially etched tap. Figure 3.10 shows a SEM photo of a completed tap, made using KOH as the etchant.

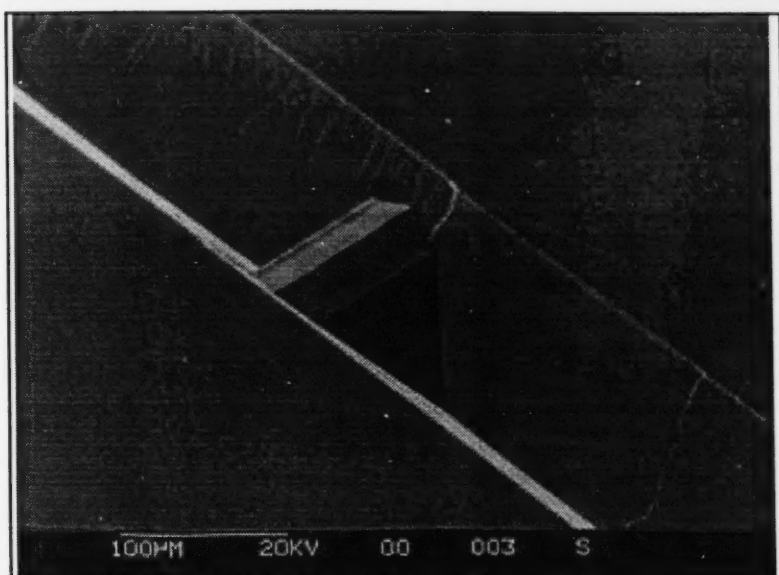


Figure 3.9 - SEM photo of partially etched centre tap

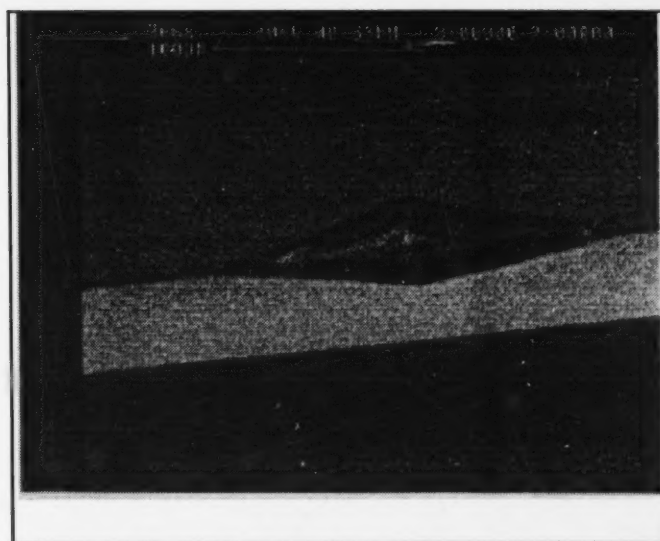


Figure 3.10 - SEM photo of finished centre tap

A difficulty arises when the tapping planes being revealed are not very steep. Table 3.1 shows the angle of incidence of rays with which tapped rays will strike the top surface of the guide, assuming they were traveling straight down the guide before they were tapped. Appendix A describes the calculations used to arrive at these figures. Any curvature in the top surface is neglected. For a core index of 1.56, only rays making angles less than the critical angle of 39.9° will be able to escape the waveguide. A $\{411\}$ plane will not tap any

light out, and a {311} plane will only tap a fraction of the light out, and the light which does escape will be traveling at a very small angle to the surface of the guide. Only a {211} or {111} centre tap is of practical value.

Tapping Plane	Angle θ	Angle of incidence with upper surface
{111}	54.7	19.4 (traveling backwards)
{112}	35.3	19.4 (traveling forward)
{113}	25.2	39.6 (traveling forward)
{114}	19.5	51.0 (traveling forward)

Table 3.1 - Angle of incidence with upper surface for various tap planes

Unfortunately, the only planes observed when attempting to make centre taps with the process described above were {411} for pure KOH and {311} for KOH/IPA mixtures. The {411} planes are to be expected for KOH, as these are also the fast-etching planes observed when undercutting convex corners. The {255} planes observed for KOH/IPA undercutting would be steeper than the slow etching {111} planes, so they cannot form. Apparently {311} is the fastest etching set of {mnn} planes steeper than {111} for KOH/IPA, at least in the 60°C to 80°C range tested here. 40% and 25% KOH/IPA solutions were also tried, in addition to the 30%, but no changes in the dominant planes were observed. Etching with EDP, as done in [13] appears to be the only way to get {211} planes for centre taps.

These results forced the abandonment of the centre tap idea, and efforts were then focused on sidewall taps. Section 5.2 describes some possible alternative techniques for fabricating centre taps, which may be investigated in future work.

3.3.2 SIDEWALL TAPS

Sidewall taps are formed by the undercutting of rectangular projections of the SiO₂ masking layer into the main waveguide mask opening. Figure 3.11 shows the mask pattern which would form 3 sidewall taps in a v-groove guide. Each of the pair of convex corners of each rectangular stub will be etched away by a pair of planes, as indicated previously in figure 3.2. At the same time, the v-groove will start to form as the main waveguide section

is etched downwards, limited by the slow etching $\{111\}$ planes which form the side walls of the guide.

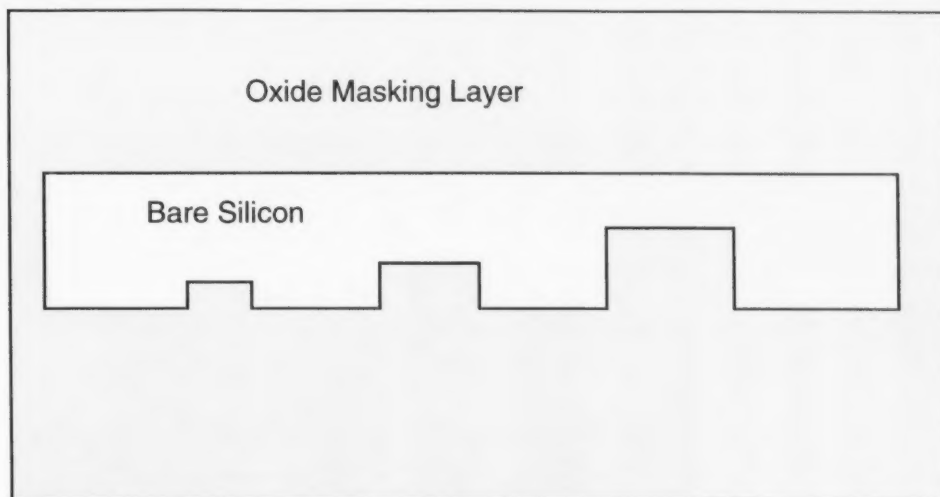


Figure 3.11 - Mask Pattern for three sidewall taps (not to scale)

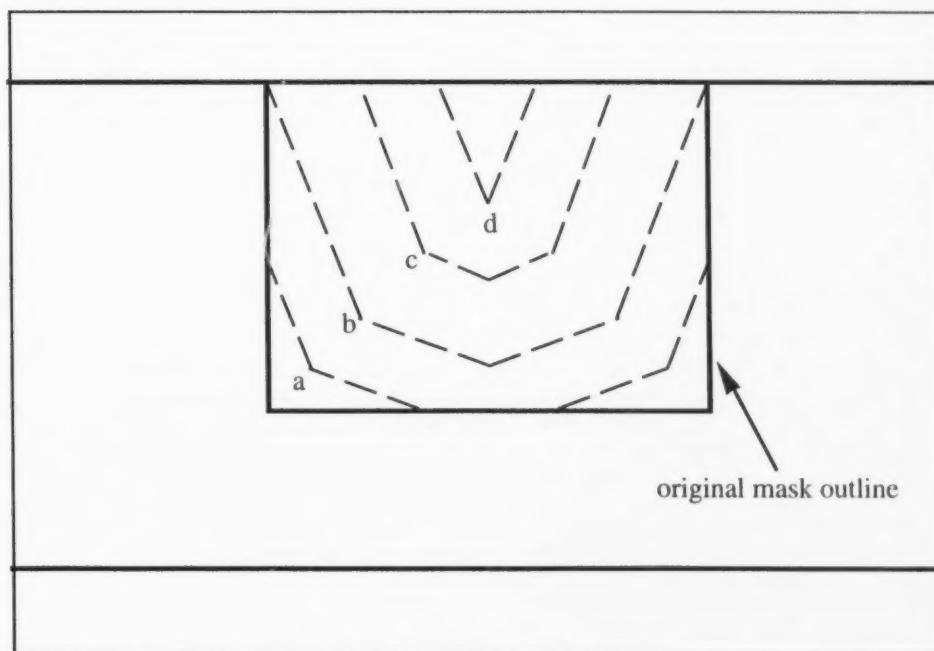


Figure 3.12 - Evolution of $\{100\}$ Si surface under mask

Figure 3.12 shows the evolution of the shape of the $\{100\}$ surface of the stub, from a to d, as the mask is undercut. Due to the symmetry of the etch rates, the intersection of the two planes at each corner will travel along a line making a 45° angle to the original mask

corner, until the two corners meet (point d). After this point, the outer {525} planes dominate the tap. Figure 3.13 is was taken with the aid of an optical microscope, and shows a partially etched v-groove and tap. The SiO₂ mask over the tap is thin enough to be fairly transparent. Figure 3.14 is a SEM photograph of a finished tap. Some residual planes may be seen between the two large {525} planes. These planes may account for some of the excess loss seen at each tap, as they scatter some of the light, but most of the light striking them will remain in the guide, as they form a fairly small angle with the waveguide axis.,

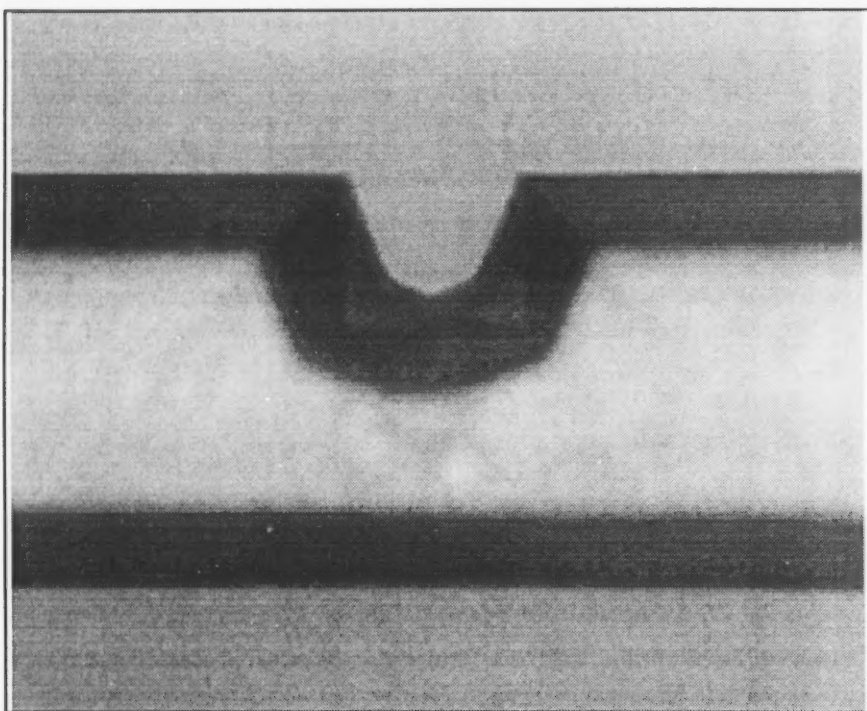


Figure 3.13 - Photo of partially etched sidewall tap

KOH/IPA was chosen as the etchant of choice for fabricating sidewall taps, as the KOH undercutting rate was too rapid to be of use. To form a 50% tap, the diagonal etch rate must be less than the square root of two times the downward etch rate. Otherwise, the required rectangular stub would have to be larger than the width of the waveguide. The goal of the experiment was to fabricate a one to five serial out-of-plane splitter. This requires four sidewall taps, tapping 1/5, 1/4, 1/3, and 1/2 of the light respectively, and an end facet which taps all the remaining light.

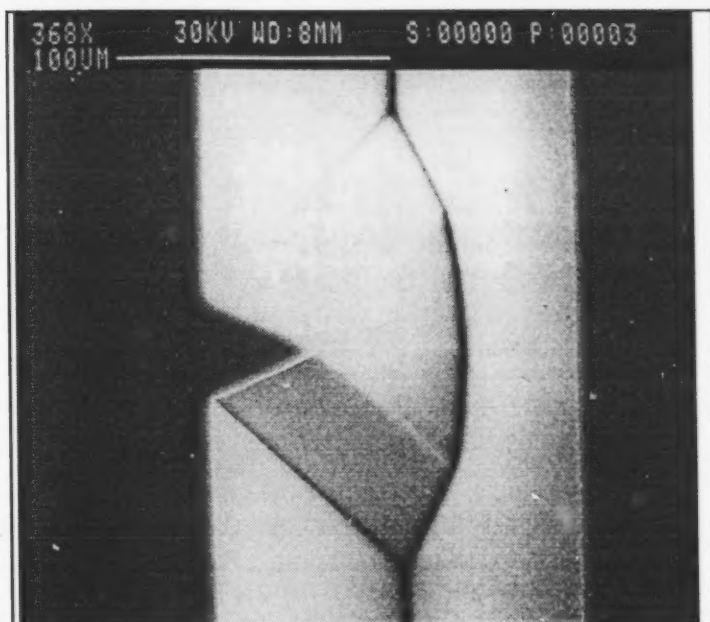


Figure 3.14 - SEM Photo of Sidewall Tap

To design the mask, some simplifications were made. Most of the taps were spaced 5mm apart, in accordance with the simulation results for eliminating shadowing effects. Other tap spacing were also tried, to investigate the real shadowing effects. It was assumed that the only plane of significance for the tap was the front $\{525\}$, and that a $\{111\}$ plane was between the front and back sides of the tap (see figure 3.14). This means that when looking down the end of the guide, the left and right sides of the tap are parallel to each other. Finally, the waveguide cross-section was assumed to be triangular. In reality, the surface tension of the polymer dispensed in the v-groove will result in a convex curve in the top surface of the waveguide core. Provided sufficient polymer is added to the guide, this curvature should be fairly small.

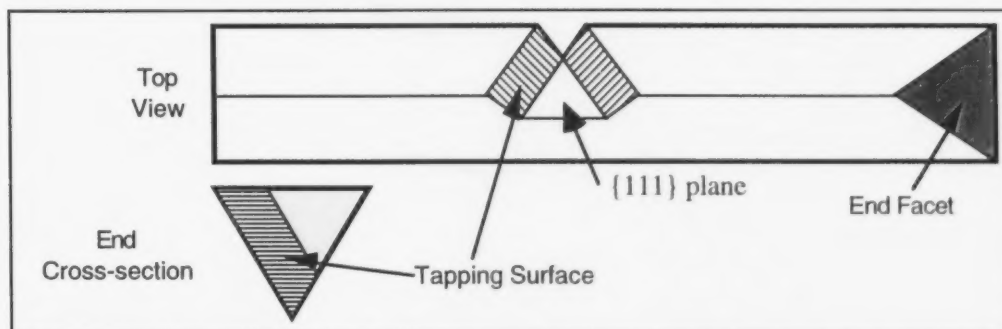


Figure 3.15 - Idealized sidewall tap

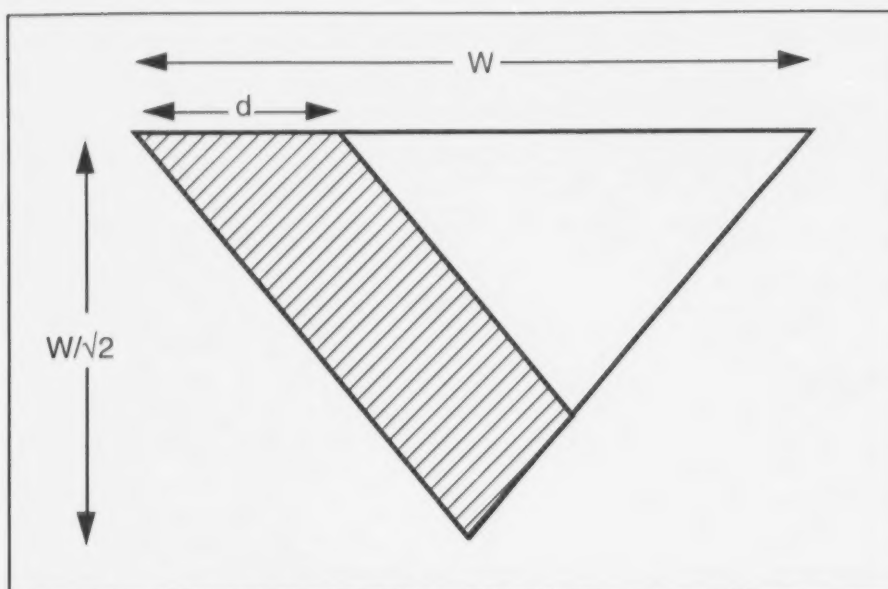


Figure 3.16 - Cross-section of idealized sidewall tap and waveguide

Given the idealized triangular geometry of the waveguide cross-section shown in figure 3.16, the desired distance "d" for a given tap ratio "R", in a guide of width "w" can be easily shown to be given by:

$$d = w \cdot (1 - \sqrt{1 - R})$$

R is defined as the ratio of the power tapped to the total waveguide power arriving at the tap. For a 1 to 5 splitter, the desired R values are 0.2, 0.25, 0.33, 0.5, and 1.0.

This design neglects shadowing effects and propagation loss. To decrease the effects of shadowing with sidewall taps, each tap can be placed on the opposite side of the waveguide as the preceding tap. This was not done on this design.

Figure 3.17 shows the geometry involved in determining the mask dimensions to achieve a given tap width "d". It is assumed that the timed etch will cease just as the exterior {525} planes meet to create a triangular shaped {100} surface under the masking layer. This simplifies the mask design, as after this point the etch ceases to move along the 45° lines from the mask corners.

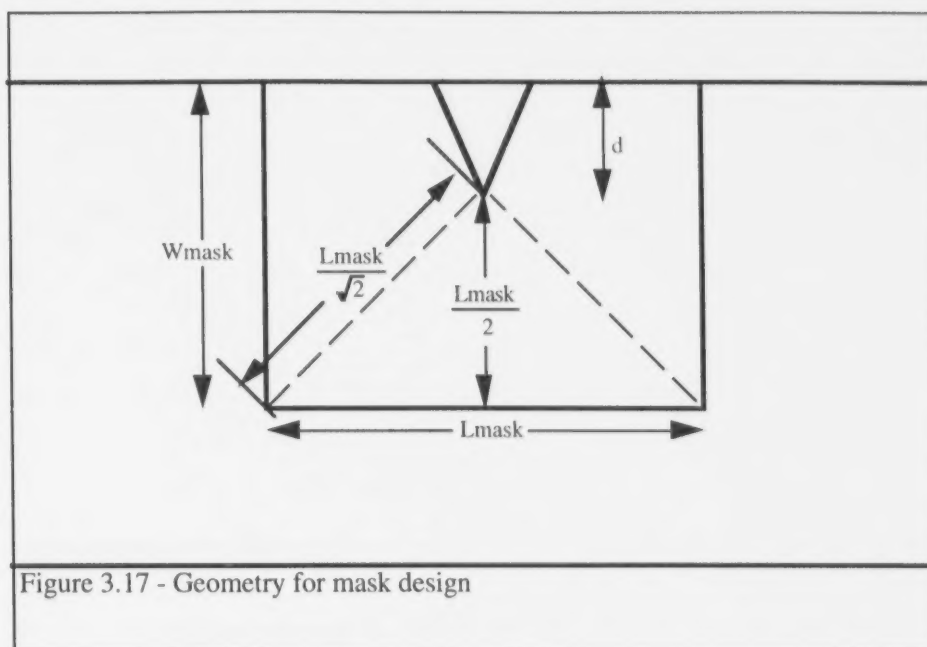


Figure 3.17 - Geometry for mask design

It was decided to have the v-grooves finish etching at the same time as the {525} planes meet. Thus the time for the diagonal distance $\frac{L_{\text{mask}}}{\sqrt{2}}$ to be etched must be the same as the time for the {111} sidewalls to meet at the bottom of the groove. The vertical depth of the groove is equal to the guide width, "w", divided by $\sqrt{2}$. Thus, having determined R_{100} , the downward etch rate, and R_{diag} , the diagonal etch rate, in section 3.2.2, it is simple to determine the following relationships:

$$L_{\text{mask}} = w \cdot \left(\frac{R_{\text{diag}}}{R_{100}} \right)$$

$$W_{\text{mask}} = d + \frac{L_{\text{mask}}}{2}$$

For $R_{\text{diag}} = 0.31 \text{ um/min.}$, and $R_{100} = 0.63 \text{ um/min.}$, and a waveguide width of 125 um , the following stub dimensions are necessary:

R	d (um)	L _{mask} (um)	W _{mask} (um)
0.2	13	61	44
0.25	17	61	47
0.33	23	61	53
0.5	37	61	67

Table 3.2 - Mask Dimensions for 1:5 split

The following chapter deals with the actual fabrication of waveguides using a mask designed with taps of these dimensions.

CHAPTER 4 - FABRICATION AND TESTING OF TAPPED WAVEGUIDES

4.1 FABRICATION OF WAVEGUIDES

4.1.1 ETCHING

A new 30% KOH solution was mixed up, and saturated with IPA, as the solution which had been used during the etch rate characterization had been contaminated with oil. This solution proved to have a virtually identical downward etch rate, but the diagonal etch rate was slightly faster. This resulted in taps which were slightly smaller than the designed size, due to overetching. This change in etch rate is likely due to a small change in the concentration of the solution. For future work, several characterization etches should be done prior to the actual waveguide etching. The concentration of the solution can be changed by adding more water or KOH, until the desired ratios are achieved.

In retrospect, a better design for the mask dimensions would be to have the v-groove finish etching prior to the completion of the tap formation. This would serve several purposes. When the $\{111\}$ planes meet at the bottom of the guide, there are still some small imperfections (micropyramids) on the surfaces of the $\{111\}$ planes, particularly at the very bottom of the grooves. If etching is allowed to continue, these micropyramids disappear, as they are made up of planes which etch faster than the $\{111\}$ sidewalls. With the present mask design, etching must stop as soon as the $\{111\}$ planes meet, or the taps will be overetched.

Another advantage would be an increased tolerance to changes in the etch ratio between the downward and diagonal directions. If the mask were designed so that there was a ten minute time difference between the completion of the v-groove and the completion of the taps, a minor increase in the diagonal etch rate could be compensated for by decreasing the etch time. Lastly, having the v-grooves finish first would lead to an increase in the size of masking stubs. This may improve the results, by reducing the error introduced by the finite resolution of the photolithography.

Another difficulty encountered during the etching process was the misalignment of the mask with the $\langle 110 \rangle$ direction. The 4" wafers being used have a tolerance of $\pm 2^\circ$ in their orientation. A significant misalignment of mask will result in steps forming in the sidewalls of the waveguide, as the $\{111\}$ planes no longer run parallel to the mask opening. If the mask is not too badly aligned, these steps are long enough that they should not add significantly to the waveguide losses. However, there are other side-effects of the

misalignment, which are more severe. The waveguide will grow wider as there is no longer a continuous {111} etch stop layer. This widening is most noticeable at discontinuities in the sidewalls, where the taps are located. Another problem is that the corner undercutting is more severe when the waveguide is misaligned. This results in undersized taps.

As a result of these problems, the wafer yield was fairly low. Of ten four inch wafers used, four had sufficient problems due to misalignment that the taps or waveguides were unusable. Three others had noticeable defects, but probably could have been used without significant problems.

The simplest solution to this problem is to use wafers with more accurate orientation. Four inch wafers with alignment tolerances of less than 0.5° are available. They are of course more expensive. Another possible solution is to fabricate exact crystallographic markings on each wafer, using an anisotropic pre-etch [53]. If several small circular openings are made in an oxide mask, and the wafer then placed for several minutes in an anisotropic etching like KOH, inverted pyramids formed by {111} planes will form in the silicon. The edges of these pyramids will be perfectly aligned with the $\langle 110 \rangle$ direction. These edges can then be used to align the mask.

4.1.2 METALIZATION OF TAPS

An issue of significance is how to metalize the tapping planes, to improve their reflectivity. The simplest approach is to coat the entire wafer with metal after the waveguides have been etched. A SiO_2 cladding layer can be deposited on top of the metal, using CVD. The cladding layer keeps the light away from the lossy metallic surface, until the tapping plane is encountered. Light which is not reflected at the core/cladding interface will pass through the cladding, and be reflected by the metal. This procedure requires no additional masking steps, which simplifies the processing considerably.

This method has been tried in the past [54,55], but not without experiencing some problems. A highly reflective metal film, such as silver or aluminum, is desired. Unfortunately, these metals do not stand up well to the CVD oxidation process. Small bubbles tend to form in the SiO_2 , which significantly degrade the reflectivity of the surface. These bubbles were attributed to a recrystallisation of the metal at elevated temperatures, which leads to the nucleated growth of SiO_2 [14]. Sputtered titanium, with its very high melting point, has shown the best resistance to the processing [55]. Unfortunately the reflectivity of Ti is fairly low, measured in [55] to be 57% at 633 nm.

An alternative approach is to place the metalization layer on top of the cladding layer. To avoid a large propagation loss due to the finite conductivity of the metal, the metal film must be placed only on the taps, and not on the rest of the waveguide. This patterning of the metal requires an additional photolithographic step, thus complicating the fabrication process.

A final possible approach would be to avoid the use of a CVD oxide cladding altogether. First a high reflective metal film could be deposited on the entire waveguide. Next, a lower index polymer could be spun-on to the v-grooves and cured, prior to the deposition of the core polymer. This would yield a waveguide cross-section similar to that shown in figure 4.1.

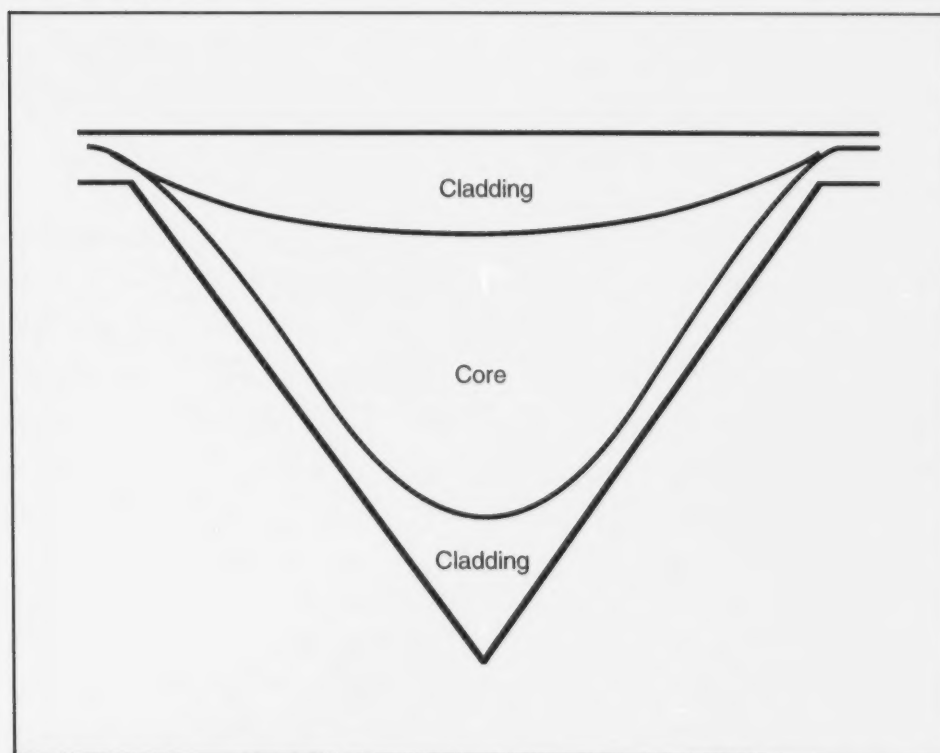


Figure 4.1 - Cross-section of waveguide with polymer lower cladding

For the testing done for this thesis, it was decided to use the simplest approach, a titanium film coated by CVD oxide technique. The polymer cladding method would reduce the cross-sectional area of the waveguide, requiring the taps to be stick out farther from the sidewall of the waveguide in order to achieve the desired one to five split. With a new mask design, this would be advantageous, as increasing the tap sizes decreases the percent error introduced by inaccuracies in the lithography.

A 0.1 micron thick sputtered Ti film was used as the reflective coating. Preliminary testing indicated that a smooth SiO₂ layer could be deposited on this film. However, when final waveguide fabrication was done, some samples showed the presence of bubbles in the oxide layer. As these bubbles were not visible in wafers from the first run, and different wafers had greatly different densities of these bubbles, it is suspected that these can be avoided by careful processing. Wafer cleanliness may have been a problem, as the second batch of wafers had been etched more than two days before the Ti deposition, whereas the first run was done on freshly etched wafers. For the sample used in the tap measurements in section 4.3, the reflection loss measured at a 45 degree angle of incidence was between 4.8 and 5 dB. This loss will result in a high excess loss for each tap. The rougher tap surface will also scatter the light, making it more difficult to collect with a pickup fiber positioned over the tap.

4.1.3 DEPOSITION OF CORE AND CLADDING LAYERS

The lower SiO₂ cladding layer, which serves to isolate the propagating light from the lossy silicon, was deposited using CVD. A thickness of 3 microns was used. This was slightly thicker than the 2.6 μm layer found by Kumar [14] to give minimum propagation loss in his v-groove waveguides.

After the CVD SiO₂ buffer layer is grown, the waveguide core must be deposited. The core consists of a UV curable optical adhesive, made by Norland. This adhesive, NOA 81, has a refractive index of 1.56. The liquid polymer is dispensed in the waveguide through the use of a computer controlled system developed at TR Labs. The polymer is placed in a syringe, with a 50 μm diameter tip. The etched silicon wafer is placed on a vacuum chuck, on a platform which is movable by a computer controlled x-y micropositioner. The syringe is held in a clamp attached to another computer controlled micropositioner, which travels in the vertical, or z, direction. The user enters the desired speed of travel and using a joystick indicates the start and endpoints of the waveguide. All the subsequent steps are controlled by the computer. The syringe tip is positioned one end of the waveguide and lowered slightly into the v-groove. It then begins to move along the waveguide, towards the opposite end. As the tip begins to move, compressed air is pumped into the syringe, forcing polymer into the v-groove. The flow is stopped when the end of the waveguide is reached. With a proper choice of tip speed and air pressure, the waveguide can be filled almost to the top. The meniscus caused by the surface tension in the polymer gives a very smooth, curved top surface to the core.

A large number of trials were performed, using different dispensing speeds and pressures. It was found that for NOA 81, with a 50 μm diameter syringe tip, the best results were obtained using a speed setting of 45 and a pressure of 36 psi. Dispensing one 4.5 cm long waveguide core takes approximately 20 seconds at this speed setting.

After the core has been dispensed in all the waveguides on the wafer, the wafer is placed in an EPROM eraser, which irradiates the polymer with UV light. Cure times of 50 minutes were used, to ensure complete curing of the core. Next, another polymer was dispensed on top of the core to act as an upper cladding layer. Norland NOA 68, which has an index of 1.54, was used for this cladding. A dispensing speed of 32, at 36 psi was found to fill the waveguide so that it is level to the surface of the silicon wafer. This cladding layer is then cured in the EPROM eraser as well. Figure 4.2 shows a photo of the cross-section of a completed waveguide.

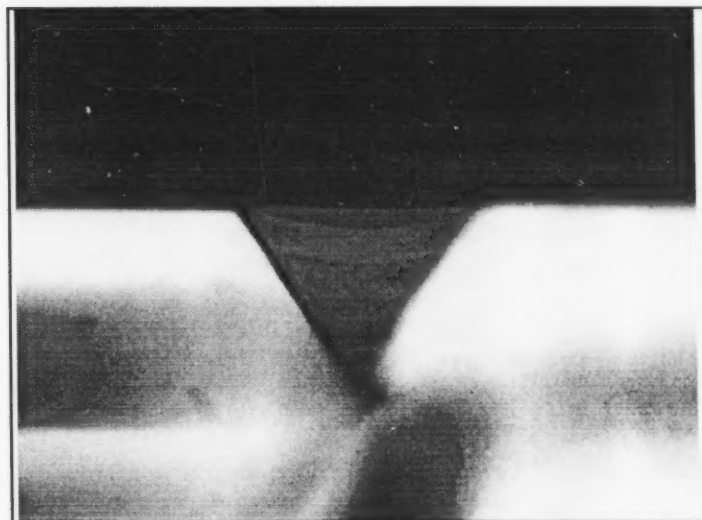


Figure 4.2 - Cross-section of completed v-groove waveguide

In order to couple light into the waveguide, the input end of the waveguide must be cleaved. Some problems were encountered when cleaving the wafers. The polymer would often not break cleanly at the cleave, leaving a jagged, unusable input facet. Occasionally, the polymer would not break at all, and the whole waveguide would peel out of the v-groove. To solve this problem, the wafers are placed in a freezer for ten minutes prior to cleaving. This renders the polymer much more brittle, and the waveguides cleaves much more cleanly. Once the wafers are cleaved, they are ready to be used as serial out-of-plane waveguide splitters.

4.2 WAVEGUIDE TESTING

For testing the waveguides, a 675 nm laser was used. A 1 meter length of single mode fiber was connected to the laser using an FC connector, and butt-coupled to the input facet of the waveguide under test. Output light was measured using a 40 cm long, 1 mm diameter core pickup fiber. The output of this fiber was directed onto the large area detector head of an optical power meter. The zero dB reference power for all measurements was taken as the power measured when the input fiber was butt-coupled to the pickup fiber. This power was approximately 1 mW.

Two different tests were performed on the waveguides. The first was a cut-back loss measurement, done on two waveguides from the same wafer. These waveguides had no taps in them. The end-facet of each waveguide was cleaved off, and the output power of each waveguide was measured. Next, a short section of the end of the wafer was cleaved off, and the power remeasured. This process was repeated several times. For an ideal cut-back loss measurement, the input fiber should be pigtailed to the waveguide under test, to ensure that the input conditions don't change. In the interests of expediency, this was not done for this measurement. However, the input fiber was adjusted with a three-axis micropositioner to maximize the output power before each measurement, so it is unlikely that there was a significant change in the insertion loss. The results of the cutback measurements are shown in figure 4.3, along with linear fits to the two data sets.

The intersection of the straight line with the zero distance axis gives the insertion loss of the guide. In this case the insertion losses are 1.3 and 0.9 dB. The slope of the line indicates the propagation loss, here 1.0 and 1.1 dB/cm. This propagation loss is similar to the 0.5 to 1.6 dB/cm loss measured by Kumar [14]. There is some uncertainty in these loss measurements, as the linear fit is not perfect. This is in part due to the fact that a significant portion of the loss is due to large scattering centres, which are not uniformly distributed throughout the waveguide. Scattered light is visible all along the length of the waveguide, but some spots much brighter than the background. These bright spots are due to imperfections in the etching of the v-grooves. As mentioned in section 4.1, the number of these micropylramids can be greatly reduced by etching the guides for a slightly longer period of time. The bubbles in the SiO₂ mentioned in section 4.2 are also a scattering source, although less significant.

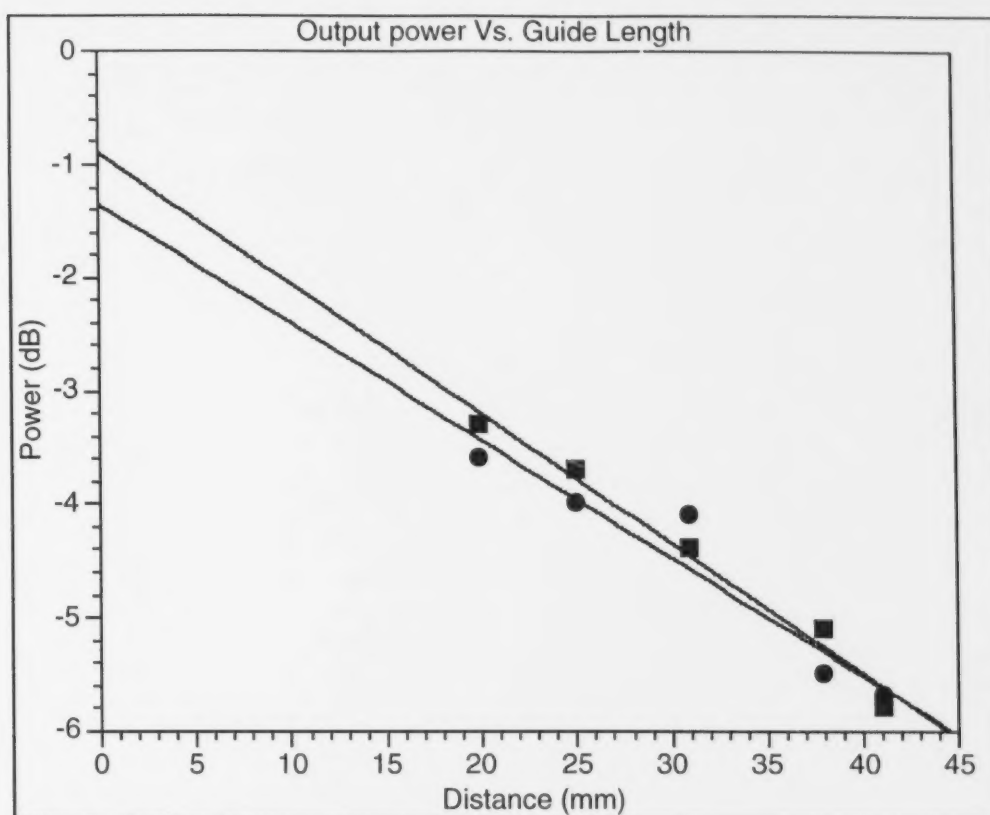


Figure 4.3 Cutback measurement results

The second test made on the waveguides was a tapped power measurement. Four waveguides were tested, each with 4 sidewall taps designed to give an even 1 to 5 split of the light. Each waveguide had a different spacing between the taps. Spacings of 1 mm, 3 mm, 5 mm, and 7.5 mm were used. There was a 9 mm separation between the input facet and the first tap. The large core pickup fiber was positioned above the waveguide surface, to collect the tapped light. The angle of the fiber was adjusted so that a maximum amount of light would be picked up. This angle is different for the end facet than it is for the rest of the taps. The input fiber was positioned to maximize the amount of light coming from tap number 2, and then held fixed while all the other taps were measured. The results for these measurements are summarized in the bar graphs of figure 4.4.

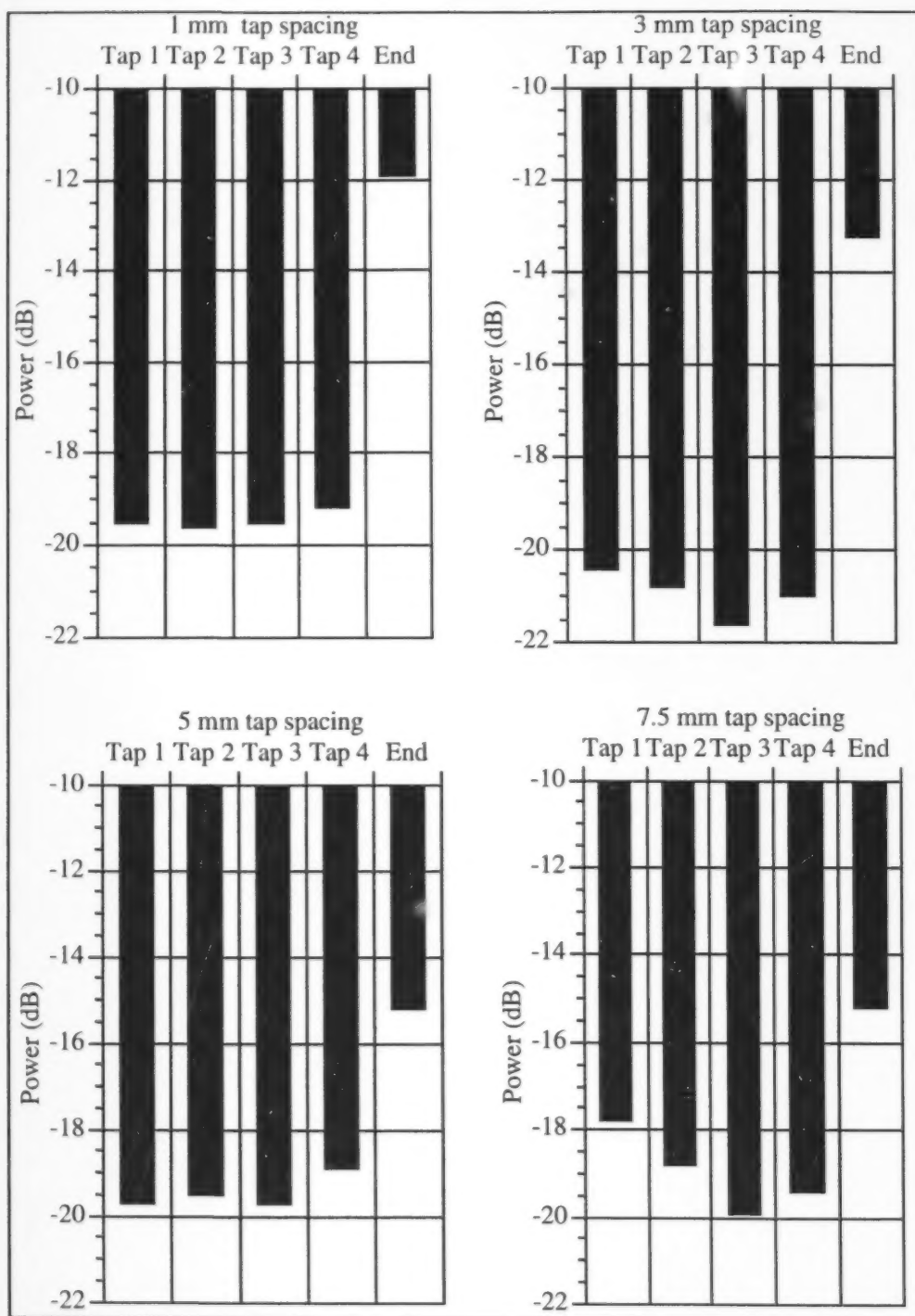


Figure 4.4 - Tapped Power Results

Several comments can be made regarding these results. An ideal 1 to 5 splitter (four taps and one end facet) should have a -7 dB output at each tap. The typical output power from the sidewall taps was 12 to 14 dB worse than this figure. This difference can be attributed to several reasons. There is significant reflection loss at each tap due to the intrinsic properties of the titanium and the presence of imperfections in the oxide layer. At a 45° angle of incidence, the reflection loss was measured as 4.8 to 5 dB. There was a 6 to 7 dB difference between the power measured reflecting from the end-facet and the power measured at the end of the guide when the end facet was cleaved off. This implies that the loss due to the pickup fiber not collecting all the light from the end facet is approximately 1 dB. Adding a drop of index matching fluid to the end of the pickup fiber reduced the divergence of the rays exiting the guide and increased the measured power by 0.9 dB. This situation is probably even worse at the sidewall taps, as the rays are exiting at a steeper angle. A better method of measuring the tapped power, such as a flat photodiode moved along the guide, or a photodetector array, would probably give a better indication of the true tapped power.

Another source of the large difference between the measured and ideal tapped powers is that the waveguide design assumes no propagation or coupling loss. There is actually a propagation loss of approximately 1.0 dB/cm, and another 1.1 dB of insertion loss.

The calculation of a more realistic tapped power value, rather than the -7 dB expected for an ideal waveguide is shown below, for the first tap of the waveguide.

Power reaching tap = P_{in} - Insertion Loss - distance to tap * propagation loss

Tapped power = Power reaching tap * ratio of tap to guide areas - reflection loss

Measured power = Tapped power - loss in collecting light in pickup fiber

For a waveguide with 1.1 dB insertion loss, 1.0 dB/cm propagation loss, 9 mm distance between the input facet and the first tap, a 5 dB reflection loss and a 3 dB loss in collecting the output light, the expected measured power of a tap designed to reflect -7 dB would be:

$$0 \text{ dB} - 1.1 \text{ dB} - 0.9 \text{ dB} - 7 \text{ dB} - 5 \text{ dB} - 3 \text{ dB} = -17.0 \text{ dB}$$

Table 4.1 shows the measured data compared to what would be expected, taking into account an estimate of the insertion, propagation, reflection, and coupling losses (loss due to not coupling all reflected light into the pickup fiber). The difference between the measured

and expected values are given as the excess loss for the tap. The reflection loss is assumed to be 5 dB, and the coupling loss to be 1 dB for end facets and 3 dB for the sidewall taps. The 3 dB loss collecting light from the sidewall taps is somewhat arbitrary, but not unreasonable given the fact that the light will be scattered by the rough tapping surface (see section 4.1.2).

Guide number	Tap Spacing	Tap Number	Measured Pow. (dB)	Expected Pow. (dB)	Excess Loss (dB)
1	1 mm	1	-19.5	-17.0	2.5
		2	-19.6	-17.2	2.4
		3	-19.5	-17.3	2.2
		4	-19.2	-17.5	1.7
		5	-11.9	-15.6	-3.7
2	3 mm	1	-20.4	-17.0	3.4
		2	-20.8	-17.4	3.4
		3	-21.6	-17.7	3.9
		4	-21.0	-18.1	2.9
		5	-13.2	-16.4	-3.2
3	5 mm	1	-19.7	-17.0	2.7
		2	-19.5	-17.6	1.9
		3	-19.7	-18.1	1.6
		4	-18.9	-18.7	0.2
		5	-15.2	-17.2	-2.0
4	7.5 mm	1	-17.8	-17.0	0.8
		2	-18.8	-17.8	1.0
		3	-19.9	-18.6	1.3
		4	-19.4	-19.4	0.0
		5	-15.2	-18.2	-3.0

Table 4.1 - Comparison of measured tap powers and theoretical values

Another source of excess loss is that the actual taps are smaller than they should be. Not only are the taps slightly overetched due to the increase in the undercutting rate, but the design did not consider the decrease in the waveguide width due to the SiO₂ buffer layer of

3 microns. Having taps which are too small will have the effect of increasing the power at 100% end facet tap, at the expense of the other taps. This is definitely apparent in the excess loss data. The excess loss measured at the end facet is negative, i.e. the power at the end facet is larger than would be expected. Obviously a significant amount of power is traveling past the taps to the end facet, rather than being tapped out. Table 4.2 shows the excess loss if each tap is assumed to be 5 μm narrower than desired.

Guide number	Tap Spacing	Tap Number	Measured Pow. (dB)	Expected Pow. (dB)	Excess Loss (dB)
1	1 mm	1	-19.5	-20.0	-0.5
		2	-19.6	-18.8	0.8
		3	-19.5	-17.6	1.9
		4	-19.2	-16.6	2.6
		5	-11.9	-13.5	-1.6
2	3 mm	1	-20.4	-20.0	0.4
		2	-20.8	-19.0	1.8
		3	-21.6	-18.0	3.6
		4	-21.0	-17.2	3.8
		5	-13.2	-14.3	-1.0
3	5 mm	1	-19.7	-20.0	-0.3
		2	-19.5	-19.2	0.3
		3	-19.7	-18.4	1.3
		4	-18.9	-17.8	1.1
		5	-15.2	-15.1	0.1
4	7.5 mm	1	-17.8	-20.0	-2.2
		2	-18.8	-19.4	-0.6
		3	-19.9	-18.9	1.0
		4	-19.4	-18.5	0.9
		5	-15.2	-16.1	-0.9

Table 4.2 - Comparison of loss measurements using decreased tap size model

Shadowing effects may also be seen in these measurements. The 1 mm spaced taps show a greater amount of power at the end facet than the waveguides with longer spacings, even when the smaller propagation loss is taken into account. If the first tap were

shadowing the others, it would be expected that power which should strike the following taps will instead travel down to the end of the guide, increasing the end facet power, as we see here. The two guides which should have no shadowing, the ones with 5 mm and 7.5 mm tap spacings give the best match to the expected values.

Examining these results, it may be concluded that the idea of fabricating sidewall taps in v-grooves is a viable technique for serial out-of-plane optical distribution. While the performance of the particular taps tested here was far from ideal, given the known problems with their fabrication it should be possible to significantly improve on these results.

A solution is needed for the reflectivity problem, either by selectively depositing a highly reflective metal such as aluminum on top of the CVD oxide or by using a polymer lower cladding in place of the oxide. A new mask must be designed using the improvements recommended herein to avoid the problems of undersized taps.

Exciting the guide with a larger core, multimode fiber may yield even better results, as a better filled waveguide would avoid any problems caused by selectively exciting a small number of modes.

CHAPTER 5 - CONCLUSIONS

5.1 SUMMARY OF WORK

Several tasks were completed in this work. A computer program was created to analyze the propagation of light in straight multimoded waveguides. The program uses ray tracing to follow the path of rays along the guide. Many different waveguide geometries can be simulated. Data collected by the software can be used to analyze the amount of power tapped from the guide, to analyze how the power distribution changes due the taps, and to analyze where the power is tapped. The results of a simulation of a complex multilayer polymer waveguide with four taps in it were compared to the experimental results obtained by other researchers. There was a very good agreement between the two data sets.

The anisotropic etching characteristics of two different etching systems were analyzed. Both aqueous KOH and KOH/IPA mixtures were used. Of particular interest with regard to the micromachining of waveguide taps are the convex corner undercutting rates of these etchants and the planes revealed by the undercutting. A 30% KOH solution in the temperature range of 60°C to 80°C was found to reveal {411} planes when undercutting convex corners. This was in agreement with most of the published works in this field. The undercutting rate was very rapid, and the mixture was deemed unsuitable for the micromachining of waveguide taps. A 30% KOH mixture saturated with IPA, in temperature ranges between 60°C to 80°C, was found to reveal {525} silicon planes when undercutting convex corners. This result is different from that reported by other authors, although there is much confusion in the literature. The downward etch rate at 76°C was found to be 0.63 microns per minute, and the undercutting rate 0.31 microns per minute. The downward etch rate did not change when a new KOH/IPA solution was mixed up, but the undercutting rate increased slightly.

When a {111}-{100} convex corner is undercut, in attempts to make taps centred at the bottom of the v-grooves, KOH etchants reveal the same {411} planes seen when undercutting 90° convex corners. KOH/IPA reveals {311} planes. Neither of these planes are sufficiently steep to tap light out of the waveguide. It was concluded that KOH based etchants cannot make centre taps in the same manner as the EDP etchant.

Using the data collected regarding KOH/IPA etch rates, and the simulation results, a photomask was designed to make waveguides with four sidewall taps and a reflective end facet. Each tap was designed to reflect one fifth of the light coupled into the waveguide. These waveguides were fabricated, and tested. The waveguide losses were approximately

1.1 dB/cm. The sidewall taps were well balanced, but there was a large excess loss at each tap, and the end facet reflected several dB more power than the sidewall taps. Much of the excess loss is related to imperfections in the reflective surface of the taps. The taps were also somewhat undersized. Some suggestions were made on ways of improving these results.

5.2 RECOMMENDATIONS FOR FUTURE WORK

Several recommendations were made within the body of the text, and are repeated here.

When the mask is designed, the dimensions should be chosen such that the v-grooves finish etching before the taps. This should result in smoother sidewalls and a greater tolerance to etch rate errors.

To avoid problems brought about by misalignment with the $\langle 110 \rangle$ direction, wafers with more accurate crystallographic orientation should be used, or alignment marks should be pre-etched onto the wafers. This should increase the yield of good wafers.

Most importantly, a method of metalizing the taps must be found which provides better reflectivity. Either the present titanium / CVD oxide procedure must be refined, or a different technique used altogether. The use of a dispensed polymer buffer layer instead of CVD oxide would avoid the degradation in reflectivity caused by thermal effects.

One area for possible investigation is to attempt to make centre taps using $\{110\}$ planes as the sidewalls and taps. If a rectangular opening is used, oriented in the $\langle 100 \rangle$ direction, rather than the $\langle 110 \rangle$ direction used for this thesis, and KOH/IPA or EDP is used as the etchant, v-shaped grooves with $\{110\}$ sidewalls at 45° angles will be formed, rather than the $\{111\}$ sidewalls usually used [56]. Taps made of $\{110\}$ planes will reflect the light vertically out of the guide, simplifying its collection. As these $\{110\}$ sidewalls are fairly fast etching planes, it will be more difficult to obtain the required smoothness.

REFERENCES

1. S.E. Miller, "Integrated Optics: An Introduction", Bell System Technical Journal, Vol. 48, No. 7, pp. 2059-2069, 1969.
2. A. Yariv, Optical Electronics, 4th Edition, Saunders College Publishing, p. 585, 1991.
3. M. Nakamura and T. Ozeki, "Optoelectronic Integration and Its Impact on System Application", IEEE Journal on Selected Areas in Communications, Vol. SAC-4, No. 9, pp. 1509-1514, 1986.
4. W.J. Tomlinson and C.A. Brackett, "Telecommunications Applications of Integrated Optics and Optoelectronics", Proceedings of the IEEE, Vol. 75, No. 11, pp. 1512-1523, 1987.
5. C.H. Henry, G.E. Blonder and R.F. Kazarinov, "Glass Waveguides on Silicon for Hybrid Optical Packaging", IEEE Journal of Lightwave Technology, Vol. 7, No. 10, pp. 1530-1539, 1989.
6. R.A. Soref, "Silicon-Based Optoelectronics", Proceedings of the IEEE, Vol. 81, No. 12, pp. 1687-1706, 1993.
7. R.I. MacDonald, D.K.W. Lam, and B.A. Syrett, "Hybrid Optoelectronic Integrated Circuit", Applied Optics, Vol. 26, No. 5, pp. 842-844, 1987.
8. W.R. Imler, et. al., "Precision Flip-Chip Solder Bump Interconnects for Optical Packaging", IEEE Transactions on Components, Hybrids, and Manufacturing Technology, Vol. 15, No. 6, pp. 977-981, 1992.
9. R.I. MacDonald and E.M. Hara, "Optoelectronic Broadband Switching Array", Electronics Letters, Vol. 14, pp. 502-503, 1978.
10. Y. Kokubun and T. Baba, "Silicon Optical Printed Circuit Board for Three-dimensional Integrated Optics", Electronics Letters, Vol. 21, No. 11, pp. 508-509, 1985.
11. S.L. Chen and J.T. Boyd, "Integrated Optical Beam Splitters Formed in Glass Channel Waveguides having Variable Weighting as Determined by Mask Dimensions", IEEE Journal of Quantum Electronics, Vol. QE-18, No. 7, pp. 1072-1077, 1982.
12. L. Rosengren, L. Smith and Y. Backlund, "Micromachined Optical Planes and Reflectors in Silicon", Sensors and Actuators A, No. 41-42, pp. 330-333, 1994.
13. M.-Y. Fei, Micromachined Center Taps for Silicon V-Groove Waveguides, MSc. Thesis, University of Alberta, 1993.
14. S. Kumar, Polymer Waveguides with Taps in Silicon V-Grooves, MSc. Thesis, University of Alberta, 1992.

15. W.-T. Tsang, C.-C. Tseng and S. Wang, "Optical Waveguides Fabricated by Preferential Etching", *Applied Optics*, Vol. 14, No. 5, pp. 1200-1206, 1975.
16. J.T. Boyd and S. Sriram, "Optical Coupling from Fibers to Channel Waveguides Formed on Silicon", *Applied Optics*, Vol. 17, No. 6, pp. 895-898, 1978
17. Y.-M. Wong, et. al. "Technology Development of a High-Density 32-Channel 16Gb/s Optical Data Link for Optical Interconnection Applications for the Optoelectronic Technology Consortium (OETC)", *Journal of Lightwave Technology*, Vol. 13, No. 6, pp. 995-1016, 1995.
18. J.M. Senior, Optical Fiber Communications - 2nd Edition, Prentice-Hall, pp. 68-69, 1992.
19. B.E.A. Saleh, M.C. Teich, Fundamentals of Photonics, John Wiley and Sons Inc., p.84, 1991.
20. D. Israel, et. al, "Comparison of Different Polymeric Multimode Star Couplers for Backplane Optical Interconnect", *Journal of Lightwave Technology*, Vol. 13, No. 6, pp. 1057-1064, 1995.
21. K. Bean, "Anisotropic Etching of Silicon", *IEEE Transactions on Electron Devices*, Vol. ED-25, No. 10, pp. 1185-1193, 1978.
22. H. Seidel, L. Csepregi, A. Heuberger and H. Baumgartel, "Anisotropic Etching of Crystalline Silicon in Alkaline Solutions", *J. Electrochem. Soc.*, Vol. 137, No. 11, pp. 3612-3626, 1990.
23. M. Mehreganry, and S. Senturia, "Anisotropic etching of Silicon in Hydrazine", *Sensors and Actuators*, Vol. 13, pp. 375-390, 1988.
24. U. Schnakenberg, W. Benecke and B. Lochel, "NH₄OH-based Etchants for Silicon Micromachining", *Sensors and Actuators A*, Vol. A21-A23, pp. 1031-1035, 1990.
25. A. Merlos, M. Acero, M.H. Bao, J. Bausells and J. Esteve, "TMAH/IPA anisotropic etching characteristics", *Sensors and Actuators A*, Vol. 37-38, pp. 737 -743, 1993.
26. G. Findler, J. Muchow, M. Koch and H. Munzel, "Temporal Evolution of Silicon Surface Roughness During Anisotropic Etching Processes", *Proceedings of Micro Electro Mechanical Systems '92*, pp. 62-66, 1992.
27. A. Merlos, M.C. Acaro, M.H. Bao, J. Bausells and J. Esteve, "A Study of the Undercutting Characteristics in the TMAH-IPA System", *J. Micromech. Microeng.*, Vol. 2, pp. 181-183, 1992.
28. C. Ju and P. Hesketh, "High Index Plane Selectivity of Silicon Anisotropic etching in Aqueous Potassium Hydroxide and Cesium Hydroxide", *Thin Solid Films*, Vol. 215, pp. 58-64, 1992.
29. Fisher Scientific, "Ethylenediamine Material Safety Data Sheet", 1994.

30. S. Kumar, Polymer Waveguides with Taps in Silicon V-Grooves, MSc. Thesis, University of Alberta, pp. 16,48, 1992.
31. J.B. Price, "Anisotropic Etching of Silicon With KOH-H₂O-Isopropyl Alcohol", Semiconductor Silicon 73, H.R. Huff & R.R. Burgess, Eds., pp. 339-353, 1973
32. E. Bassous and A.C. Lamberti, "Highly Selective KOH-Based Etchant for Boron-Doped Silicon Structures", Microelectronic Engineering, Vol. 9, pp. 167-170, 1989.
33. E.D. Palik, V.M. Bermudez and O.J. Glemboki, "Ellipsometric Study of Orientation-Dependant Etching of Silicon in Aqueous KOH", J. Electrochem. Soc., Vol. 132, No. 4, pp. 871-884, 1985.
34. E.D. Palik, R. Gray and P. Klieg, "A Raman Study of Etching Silicon in Aqueous KOH", J. Electrochem. Soc., Vol. 130, No. 4, pp. 956-959, 1983.
35. D. Kendall, "Vertical Etching of Silicon at Very High Aspect Ratios", Ann. Rev. Mater. Sci. 1979, Vol. 9, pp. 373-403, 1979.
36. L.-C. Chen, M. Chen, C. Lien, and C.-C. Wan, "The Band Model and the Etching Mechanism of Silicon in Aqueous KOH", J. Electrochem. Soc., Vol. 142, No. 1, pp. 170-176, 1995.
37. M. Elwenspoek, U. Lindberg, H. Kok and L. Smith, "Wet Chemical Etching Mechanism of Silicon", Proceedings of the 7th IEEE Micro Electro Mechanical Systems Conference (1994), pp. 223-228, 1994.
38. C. Desmond, C. Hunt and S. Farrens, "The Effects of Process-Induced Defects on the Chemical Selectivity of Highly Doped Boron Etch Stops in Silicon", J. Electrochem. Soc., Vol. 141, No. 1, pp. 178-184, 1994.
39. S. Adachi, T. Ikegami and K. Utani, "Spectroscopic Ellipsometry Study of (111) and (100) Surfaces Etched in Aqueous KOH Solution", Jpn. J. Appl. Phys., Vol. 32, Pt.1, No. 10, pp. 4398-4403, 1993.
40. X.-P. Wu and W. H. Ko, "A Study on Compensating Corner Undercutting in Anisotropic Etching of (100) Silicon", Transducers '87, pp. 126-129, 1987.
41. M.M. Abu-Zeid, "Corner Undercutting in Anisotropically Etched Isolation Contours", J. Electrochemical Society, Vol. 131, No. 9, pp. 2138-2143, 1984.
42. M. Bao, C. Burrer, J. Esteve, J. Bausells and S. Marco, "Etching Front Control of <110> Strips for Corner Compensation", Sensors and Actuators A, 37-38, pp. 727-732, 1993.
43. M. Matsuoka, Y. Yoshida and M. Moronuki, "Preparation of Silicon Thin Diaphragms Free From Micropyramids Using Anisotropic Etching in KOH Solutions", Journal of Chemical Engineering of Japan, Vol. 25, No. 6, pp. 735-740, 1992.
44. B. Puers and W. Sansen, "Compensation Structures for Convex Corner Micromachining in Silicon", Sensors and Actuators A, 21-23, pp. 1036-1041, 1990.

45. R.H. Cornely and R.B. Marcus, "Formation of Silicon Micromirrors by Anisotropic Etching", *Sensors and Actuators A*, 29, pp. 241-250, 1991.
46. H. Sandmaier, H.L. Offereins, K. Kuhl, and W. Lang, "Corner Compensation Techniques in Anisotropic Etching of (100) Silicon Using Aqueous KOH", *Transducers 91*, pp. 456-459, 1991.
47. G.K. Mayer, H.L. Offereins, H. Sandmaier, and K. Kuhl, "Fabrication of Non-Underetched Convex Corners in Anisotropic Etching of (100)-Silicon in Aqueous KOH with Respect to Novel Micromechanic Elements", *J. Electrochemical Soc.*, Vol. 137, No. 12, pp. 3947-3951, 1990.
48. CRC Handbook of Chemistry and Physics 74th Edition, CRC Press, p. 15-47
49. S.-S. Tan, H.H. Han, R. Boudreau, and M.L. Reed, "Process Induced Hillock Defects on Anisotropically Etched Silicon", *Proceedings of the 7th IEEE MEMS Conference*, pp. 229-234, 1994.
50. E.D. Palik et. al., "Etching Roughness for (100) Silicon Surfaces in Aqueous KOH", *Journal of Applied Physics*, 70 (6), pp. 3291-3300, 1991.
51. H. Han, R. Boudreau, T. Bowen, S-S. Tan, and M. Reed, "Etching Defects on KOH Etched Silicon - Implementation of Silicon Bench Technology for Low Cost Packaging", *Electronic Components and Technology Conference 1994*, pp. 625-631, 1994.
52. B. Block and M. Sierakowsky, "The Use of a Certain Fluorocarbon Surfactant and Fluorocarbon Conformal Coating Improves KOH Silicon Etching Quality", Micromachining and Micropackaging of Transducers, Ed.by C.D. Fung, P.W. Cheung, W.H. Ko, and D.G. Fleming, Elsevier Science Publishing Company, pp. 125-133, 1985
53. T.L. Poteat, "Submicron Accuracies in Anisotropic Etched Silicon Piece Parts - A Case Study", Micromachining and Micropackaging of Transducers, Ed. by C.D. Fung, P.W. Cheung, W.H. Ko and D.G. Fleming, Elsevier Science Publishers, pp. 151-158, 1985.
54. S. Kumar, Polymer Waveguides with Taps in Silicon V-Grooves, Master of Science Thesis, University of Alberta, p.16, 1992.
55. R. Narendra, Phosphorus-Doped Glass Waveguides on Silicon Substrates, Master of Science Thesis, University of Alberta, p.36, 1992.
56. Y. Backlund and L. Rosengren, "New Shapes in (100) Si Using KOH and EDP etches", *J. Micromech. Microeng.*, Vol. 2, pp. 75-79, 1992.

APPENDIX A - CALCULATION OF ANGLES OF REFLECTED RAYS

A-1 REFLECTION FROM END FACET OR CENTRE TAP

Rays traveling straight down the waveguide striking an $\{mmn\}$ centre tap or end facet making angle θ with the horizontal will be reflected and strike the top surface of the waveguide with an angle of incidence of $2\theta - 90$ degrees (see figure A-1 for the geometrical interpretation). Table A-2 gives the angle of incidence with the top of the waveguide for different $\{mmn\}$ planes.

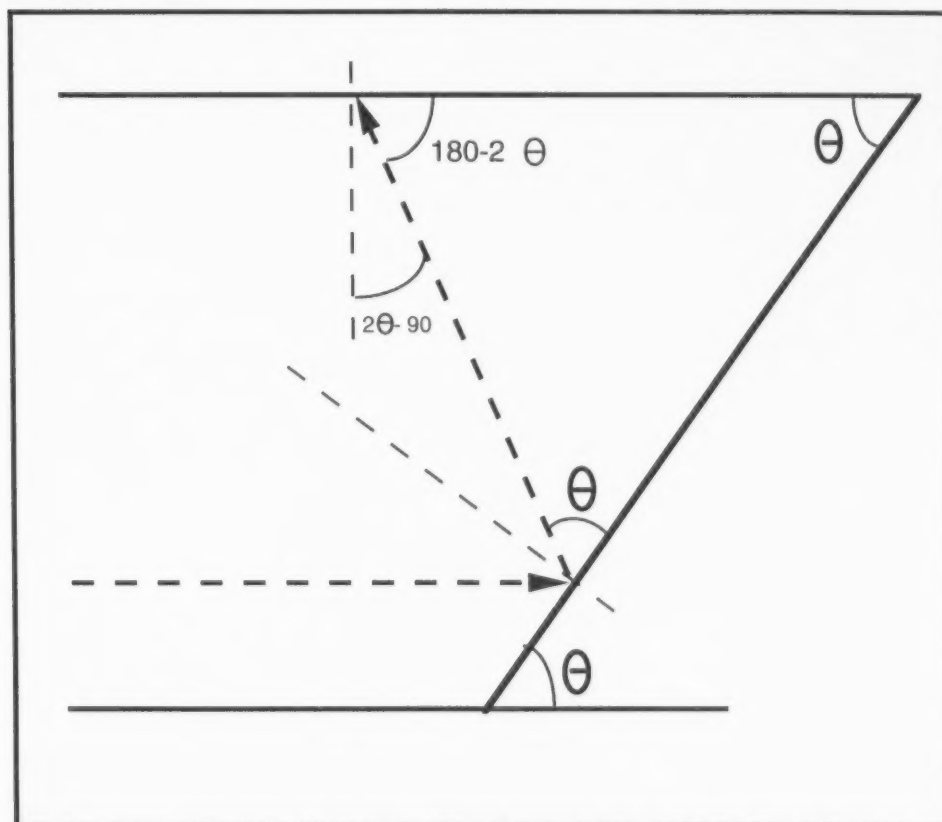


Figure A-1 - Geometrical Analysis of Ray Striking Centre Tap or End Facet

Tapping Plane	Angle θ	Angle of incidence with upper surface
{111}	54.7	19.4 (traveling backwards)
{112}	35.3	19.4 (traveling forward)
{113}	25.2	39.6 (traveling forward)
{114}	19.5	51.0 (traveling forward)

Table A-1 - Angles of Incidence of Tapped Rays on Upper Surface of Waveguide

A-2 REFLECTION FROM {525} SIDEWALL TAP

The new $\mathbf{k}$ vector of a reflected ray, $\mathbf{k}'$, may be calculated from the incident vector $\mathbf{k}$ and the surface normal $\mathbf{n}$, as follows:

$$\mathbf{k}' = \mathbf{k} - 2(\mathbf{k} \cdot \mathbf{n})\mathbf{n}$$

For a ray traveling straight down the guide, $\mathbf{k} = \left(\frac{1}{\sqrt{2}}, \frac{1}{\sqrt{2}}, 0 \right)$,

and for a {525} sidewall tap $\mathbf{n} = \left(\frac{2}{3\sqrt{6}}, \frac{5}{3\sqrt{6}}, \frac{-5}{3\sqrt{6}} \right)$

Thus, using the above equation, $\mathbf{k}' = \left(\frac{13}{27\sqrt{2}}, \frac{-8}{27\sqrt{2}}, \frac{35}{27\sqrt{2}} \right)$

The longitudinal axis of the (110) oriented waveguide runs at 45 degrees from the x or y axis. When viewed from above, the angle the ray makes with the x axis is given by:

$$\theta_x = \tan^{-1} \left(\frac{k_y}{k_x} \right)$$

Using k_x and k_y from $\mathbf{k}'$, $\theta_x = -31.6$ degrees, and since the waveguide axis is another 45 degrees further, the reflected ray makes a 76.6 degree angle with the longitudinal axis.

To find the angle the ray makes with the vertical when the waveguide is viewed from the end-on, the following formulae is used:

$$\theta_z = \tan^{-1} \left(\frac{\mathbf{k}' \cdot \left(\frac{1}{\sqrt{2}}, \frac{-1}{\sqrt{2}}, 0 \right)}{\mathbf{k}' \cdot (0, 0, -1)} \right)$$

Using $\mathbf{k}'$ in this equation yields an angle of 23.0 degrees with the vertical.

A-3 REFLECTION FROM {212} SIDEWALL TAP

The calculations for a {212} end facet are similar to those done in the previous section.

The normal vector $\mathbf{n}$ is given by:

$$\mathbf{n} = \left(\frac{1}{3}, \frac{2}{3}, \frac{-2}{3} \right)$$

Using the reflection equation,

$$\mathbf{k}' = \left(\frac{1}{3\sqrt{2}}, \frac{-1}{3\sqrt{2}}, \frac{4}{3\sqrt{2}} \right)$$

and the angles are:

$$\theta_x = 45^\circ$$

$$\theta_z = 19.5^\circ$$

APPENDIX B - SIMULATION SOFTWARE DETAILS

The simulation program was written in ANSI compliant "C" language, with no extensions used. There are actually three slightly different programs, one for v-groove guides, one for square waveguides, and one for dispensed polymer guides. The only significant differences are in how the program calculates whether a ray is inside or outside of a guide. It would be a matter of a day or so of programming to combine the three programs into one. As the principles of operation of all three versions are identical, for the purposes of this description only one program will be referred to. The program is approximately 1200 lines of code.

The simulation program takes as input two user-created data files. The first file "hwg2.in", contains information regarding the basic dimensions of the guide, the waveguide loss, the number of rays, and the rays' starting conditions. The second file, "walls.in", contains a detailed description of the waveguide. Every plane or curved surface of the guide is defined, using three or four corners, a radius of curvature, a centre of curvature, a refractive index, and information on the normal of any planes.

All output from the program is written to data files, with no messages printed to the screen, to simplify batch processing. The datafiles include cross-sectional power measurement files (one per user-defined cross-section), two histogram files containing data on the rays' angular distribution at each cross section, a waveguide power vs. distance file, and a transmitted power matrix files, which contains information on how the tapped power is distributed in the y-z plane (the top of the waveguide).

The program uses a coordinate system whereby the z-direction is down the longitudinal axis of the waveguide. In terms of the silicon Miller indices this is the $\langle 110 \rangle$ direction. The x-direction is up, normal to the wafer surface. The y-direction is horizontal, positive y being in the right direction..

The main routine of the program first loads in these two data files and stores the data in the appropriate data structures. Other data structures which will contain the simulation results are initialized. The next step is to start propagating the rays. The centre of the spot from which the rays emanate is defined in "hwg.in". It also contains beam tilt data, so that an input fiber which is not normal to the input facet can be simulated. The rays start out from points on a series of concentric circles. The spacing between these circles

increases in an exponential manner, if a Gaussian beam is desired. On each circle there are a number of ray starting points, uniformly distributed about the circle's circumference. A number of rays emanate from each of these starting points. Each ray makes a different angle with the meridional axis of the guide, creating a cone of rays emanating from these points. The angular distribution of the rays is uniform throughout the cone, unless a Gaussian beam is desired, in which case the angular distribution is Gaussian. The program loops through the rays one at a time, calculating the starting position and an initial propagation direction unit vector "k". Next, the program checks to see if this ray is starting inside the core of the guide. This is trivial for square or triangular shaped guides, but more involved for cores made by the intersection of several circles of different radii and centres of curvature, as occurs for dispensed polymer guides. If the ray is inside the guide, the starting position and k vector is passed on to the "propagate_ray" subroutine. If it is outside the guide, the program goes on to the next ray. The propagate ray routine, described below, exits when the ray has left the guide or been attenuated below a certain level. The main program will then go on to the next ray. After a certain number of rays have been finished, a message is sent to the main output file, indicating the program status. When all the rays have been propagated, the program saves all the data to the appropriate data files, through a series of subroutine calls.

The "propagate_ray" routine takes as its arguments the starting position and k vector of the current ray. The ray is assigned x, y and z electric field components appropriate for the user defined polarization and the direction of propagation. It uses the "new_xyz" routine to calculate where and on what wall this ray will strike next. The distance to this new position is used to calculate the reduction in the ray power due to the propagation loss. The total waveguide power as a function of distance array is updated to include the contribution of this ray. If the wall struck was a user-defined cross-sectional plane, the power of the ray is added to the entry in the cross-sectional power matrix appropriate for its x-y position, and the ray is allowed to continue to propagate in a straight line. Otherwise, a core boundary wall was hit, and the "reflect ray" routine is called to calculate the new k vector and to update the E-field information after a Fresnel reflection. If the boundary struck was the top of the waveguide, the loss due to reflection is equal to the power tapped out of the guide, and the tapped power is added to the transmitted power matrix in the appropriate entry for the y-z position of the reflection. Provided the reflected power is larger than a threshold level, the routine loops back to the start and calls new_xyz again. If the power is below the threshold, control is returned to the main routine, to start the next ray.

The "new_xyz" routine calculates which wall a ray with a given starting position and k vector will strike. Every wall in the waveguide is checked, one at a time. Ordinary linear vector algebra is used to calculate the length of the line in the k -direction between the starting point and the wall being checked. If this distance is positive, and less than the shortest valid distance previously measured, the intersection is checked for validity. This must be done because the distance calculation assumes all planes and curved walls are infinite, whereas in reality they exist only inside the guide, and in the case of tapers, only for a subsection of the area inside the guide. Using the information of the corners and curvature of the wall, it is determined if the ray has in fact struck a real wall or simply the infinite extension of this wall. If the intersection is valid, the distance is set as the closest distance so far, and the position and normal vector of the wall at the point of intersection are recorded, in case this is in fact the closest wall. The program then loops around and checks the next wall. After all the walls have been checked, the distance, xyz position and wall normal are returned to the calling routine, "propagate ray".

The "reflect ray" routine calls upon a number of subroutines to determine the new k and E vectors of the reflected ray, and uses the E vector to calculate the updated ray power. It receives as parameters the incident k and E vectors and the wall normal. The E vector is resolved into TE and TM components, and the Fresnel reflection formulae are used to calculate the reflected TE and TM values. The index of refraction given in the wall data file is used in this calculation. The E components and refractive index values are complex numbers, so that metallic boundaries can be used. The new k -vector is calculated using linear algebra and the law of reflection. The reflected TE and TM values are converted into a new E vector. The new power of this field is calculated. If the wall was the top surface of the guide, the transmitted power is calculated, so that the transmitted power matrix can be updated. The new k , E , and power values are returned to "propagate_ray".

The size of the data files generated by the program can become quite large, particularly if a high resolution is wanted for the cross-sectional and transmitted power matrices. A typical 3 cm x 200 μm x 300 μm dispensed guide, with ten 1 μm x 1 μm cross-sectional grids and a 1 μm x 0.1 mm transmitted power grid will generate about 12 Mbytes of data.

APPENDIX C - LITHOGRAPHY PROCEDURES

The steps involved in generating the required mask patterns on the silicon wafers prior to anisotropic etching are as follows:

1 - Thermal Oxidation

Bare silicon wafers are placed in a Mini-Brute furnace, heated to 1100°C. Nitrogen is bubbled through a flask of deionized water heated to 92°C, which causes steam to flow into the furnace, onto the wafers. After 75 minutes, the wafers are removed, and are shuffled and rotated to improve the uniformity of the growth. After another 75 minutes of oxidation, the wafers are removed. This process yields approximately 0.6 microns of oxide.

2 - Vapour Prime

The wafers are primed with HMDS to improve the adhesion of the photoresist to the oxide. This step is performed automatically in the YES vapour prime oven, and takes approximately 45 minutes.

3 - Photoresist Spin-On

The wafers are coated with Shipley HP504 positive photoresist. They are spun for 5 seconds at 500 RPM to spread the resist, and 17 seconds at 3500 RPM to obtain a photoresist layer approximately 1.5 microns thick.

4 - Photoresist Softbake

The freshly coated wafers are softbaked for one minute on a 110°C hot plate, with a vacuum applied for 50 seconds, followed by 10 seconds of nitrogen backfill.

5 - Mask Alignment and Exposure

The wafer is placed in the Suss mask aligner, along with the photomask. The alignment marks on the mask are lined up with the primary wafer flat, to ensure proper alignment of the waveguides with the (110) directions. The photoresist is then exposed for approximately 5 seconds to UV light shining through the mask.

6 - Photoresist Development

The exposed photoresist is developed using Shipley 354 developer. After a 5 second pre-wet using deionized water, the rotating wafer is sprayed with developer for 60 seconds, followed by a 90 second rinse and a 30 second spin-dry cycle.

7 - Hardbake

The developed wafers are hardbaked in an oven at 130°C for one hour, to harden the remaining photoresist.

8 - Oxide Etch

The exposed SiO₂ is etched away from the wafer using a 10:1 buffered oxide etch (BOE) (hydrofluoric acid and) at room temperature. Etch rate is approximately 0.055 microns per minute, so a 12 minute etch time is used. The wafers are rinsed and dried, and are now ready for anisotropic etching.